

**PRELIMINARY COURSE OUTLINE**  
**PHYSICS 116B: INTRODUCTION TO DIGITAL ELECTRONICS**  
**WINTER 2005**

**Class meets** MWF 1:10-2:00 PM in 158 Roessler

**Lab meets** W 3:10-6:00 PM in 152 Roessler.

Week	Monday	Topics/Notes	Lab
1	(Jan 3)	Intro; comparator, Schmitt trigger, etc. <b>First day of class</b> is Wednesday, Jan. 5	---
2	Jan 10	Pulse circuit analysis; Laplace transform	10: Schmitt Trigger
3	Jan 17	<i>M.L. King holiday on Monday</i> Logic gates and Boolean algebra <i>(Monday classes meet on Fri., Jan.21)</i>	11: Relaxation Oscillator
4	Jan 24	Combinational circuit design Logic circuits: TTL, CMOS, ECL	12: Combinational logic
5	Jan 31	Flip-flops and counters <b>Exam 1</b> on Friday, Feb. 4	13: Inside Digital IC's
6	Feb 7	Sequential circuits	14: Sequential Logic
7	Feb 14	Analog to Digital and Digital to Analog Conversion	15: A to D, D to A conversion
8	Feb 21	<i>Presidents' Day holiday on Monday</i> M68000 Microcomputer, Assembly Language, I/O	16: Tristate Busses and Memory
9	Feb 28	<b>Exam 2</b> on Wednesday, March 2	17: M68000 Assembly Language
10	Mar 7	Intro. to discrete signal analysis and FFT	18: Basic M68000 I/O (via SCSI Port).
11	Mar 14	<b>Last 116B class</b> is Monday, March 14	

**Final Exam: Friday, March 18, 10:30 AM - 12:30 PM**

Instructor: David Pellett

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Lab TA: Andrew Baldwin

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*Office Hours:* TBA

Text:

Bobrow, **Fundamentals of Electrical Engineering, 2nd ed.**

References:

Ford and Topp, **Macintosh Assembly System** (lab copies to loan)

Motorola, **M68000 Family Microprocessor User's Manual**

Motorola, **M68000 Family Programmer's Reference Manual**

plus library references and supplementary handouts

Grading: 18% MT1, 18% MT2, 25% Lab(*required, on time*), 10% HW, 29% Final.

Assignment 1 (problems due Wednesday, 1/12/04):

**Read** Bobrow, Ch. 10: Sec. 10.5; Ch. 3 (response of circuits to pulses: particularly secs 3.3 and 3.4); Ch. 5: 5.5-5.7 (Laplace transform circuit analysis); Ch. 7: 7.3 (BJT cutoff and saturation; emitter-coupled Schmitt trigger; switching time).

**Problems:** Ch. 10: 10.70, 10.71, 10.78(a), 3.29 (*assume the voltages and currents have reached their steady-state values before the switch is opened*), 3.42 (*assume the voltage across the capacitor and the current through it are zero just before the pulse arrives; you can use Thevenin's theorem here for the voltage source and two resistors*).