COURSE OUTLINE *(v. 1.01 1/5/2007)*

PHYSICS 116B: INTRODUCTION TO DIGITAL ELECTRONICS - WINTER 2007

Class meets MWF 1:10-2:00 PM in 158 Roessler

Labs meet M or W 3:10-6:00 PM in 152 Roessler.

Week	Monday	Topics/Notes	Lab
1	(Jan 1)	Intro; comparator, Schmitt trigger, etc. **First day of class** is Wednesday, Jan. 3	No lab Week 1. Lab schedule is **offset** Weeks 3-8
2	Jan 8	Pulse circuit analysis; Laplace transform	10: Schmitt Trigger
3	Jan 15	*M.L. King holiday on Monday* Logic gates and Boolean algebra *(Monday classes meet on Wed., Jan 17)*	11: Relaxation Oscillator (M: Jan 17, W: Jan 24) *(Labs meet different weeks)*
4	Jan 22	Combinational circuit design Logic circuits: TTL, CMOS, ECL **25 Min. Quiz 1** Friday, Jan. 26	12: Combinational logic (M: Jan 22, W: Jan. 31)
5	Jan 29	Flip-flops and counters	13: Inside Digital IC's (M: Jan 29, W: Feb 7)
6	Feb 5	Sequential circuits **Exam** Friday, Feb. 9	14: Sequential Logic (M: Feb 5, W: Feb 14)
7	Feb 12	Analog to Digital and Digital to Analog Conversion	15: A/D, D/A conversion (M: Feb 12, W: Feb 21)
8	Feb 19	*Presidents' Day holiday on Monday* Data Bus, memory, microcomputers	*(Wed. lab does Lab 15)*
9	Feb 26	**25 Min. Quiz 2** on Fri., March 2 M68000 Assembly Language, I/O	16: Tristate Busses and Memory
10	Mar 5	Intro. to sampled signals	17: M68000 Assembly Language
11	Mar 12	**Last 116B class** is Wed., March 14	18: Basic M68000 I/O

Final Exam: Saturday, March 17, 8:00 AM – 10:00 AM

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Lab TA: Solomon Obolu
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Texts:
Bobrow, **Fundamentals of Electrical Engineering, 2nd ed.**
Horowitz and Hill, **The Art of Electronics, 2nd ed.**

References:
Ford and Topp, **Macintosh Assembly System** (lab copies to loan)
Motorola, **M68000 Family Microprocessor User's Manual**
Motorola, **M68000 Family Programmer's Reference Manual**

Grading: 9% Quiz 1, 18% MT, 9% Quiz 2, 25% Lab*(required, on time),* 10% HW, 29% Final.

Assignment 1 (problems due Friday, 1/12/07):
Read Bobrow, Ch. 10: Sec. 10.5; Ch. 3 (response of circuits to pulses: particularly secs 3.3 and 3.4); Ch. 5: 5.5-5.7 (Laplace transform circuit analysis); Ch. 7: 7.3 (BJT cutoff and saturation; emitter-coupled Schmitt trigger; switching time).
Problems: Ch. 10: 10.68, 10.73, 10.78(a), 3.29 *(assume the voltages and currents have reached their steady-state values before the switch is opened),*
3.42 *(assume the voltage across the capacitor and the current through it are zero just before the pulse arrives; you can use Thevenin's theorem here for the voltage source and two resistors).*