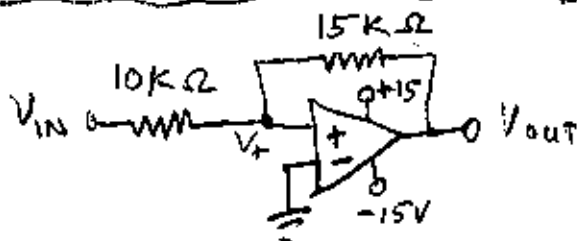


closed book and notes except for one $8\frac{1}{2}$ " x 11" sheet.
 Show reasoning for full credit. There are 6 probs / 100 pts

20

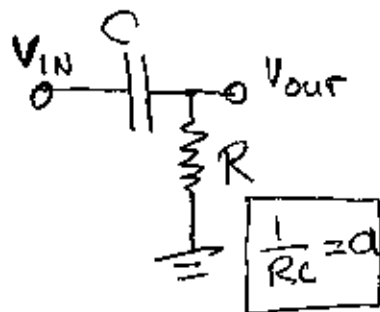
1. Assume that the output voltage limits are $\pm 15V$ for the op-amp.



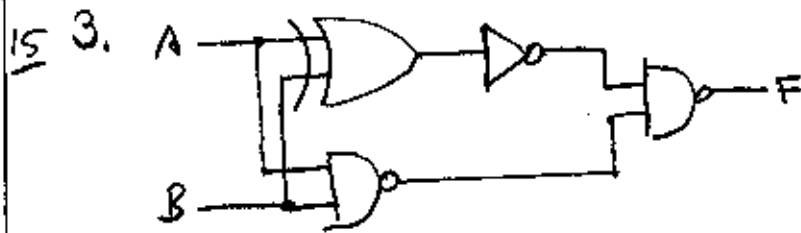
- Find V_+ and V_{out} when $V_{in} = -15V$.
- V_{in} is now increased toward $+15V$. Find the threshold voltage for the output voltage to change and the new output voltage after the threshold is crossed.
- Explain why the output voltage changes rapidly after the threshold is crossed.
- Sketch the curve of V_{out} vs. V_{in} over the range of V_{in} between $-15V$ and $+15V$, for V_{in} both increasing and decreasing. (i.e., sketch the transfer characteristic). Explain what is meant by hysteresis.

20

2. A pulse, $V_{in} = V_0(1 - e^{-at})u(t)$ is input to the RC circuit shown. R and C for the network are chosen such that $\frac{1}{RC} = a$. Refer to the table of Laplace transforms.



- Find $H(s)$ for the network.
- Find $\hat{V}_{in}(s)$.
- Find $\hat{V}_{out}(s)$, assuming the voltages and currents are zero for $t < 0$.
- Find $V_{out}(t)$.



(a) Write down the logical function, $F(A,B)$, implemented by the circuit above. (i.e., just transcribe the circuit diagram into a logical expression).

(b) Use theorems of Boolean algebra to simplify the expression.

(c) Implement the simplified expression using nands and inverters.

(d) Can this be implemented using a single 7400 chip (quad 2-input nand)? If so, how?

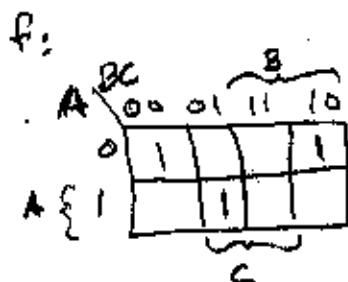
15 4. (a) Make a Karnaugh map of the function,

$$F(A,B,C) = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + ABC$$

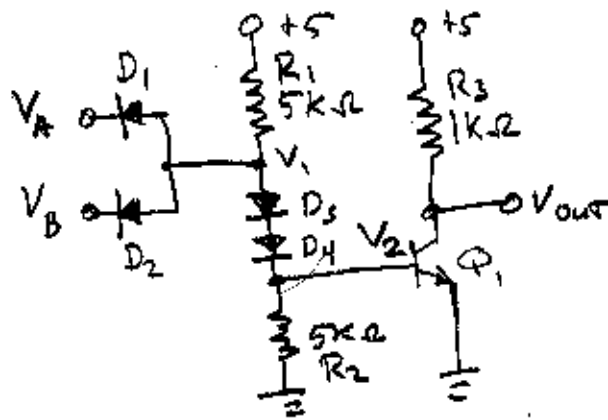
(b) Use the Karnaugh map to simplify the fun.

(c) Could this be implemented using a single, fairly common gate?

10 5. Simplify the function in the Karnaugh map below. Express the function in simplified sum-of-products form and implement with nands and inverters.



can use
3-input nands



This is a diode-transistor logic (DTL) gate. Assume that the diodes have a forward voltage drop of $0.7V$ and require more than $0.5V$ forward bias for substantial current to flow.


(a) Let $V_A = +5V$ and $V_B = +5V$ (both inputs "true"). This means D_1 and D_2 are both reverse biased and current flows through R_1 , D_3 and D_4 to pull up the voltage, V_2 , on the base of Q_1 . Assume this is sufficient to bring the silicon BJT into saturation. Estimate V_2 and V_{out}

(b) Now set $V_A = +5V$ ("true") and $V_B = +0.2V$ ("false"). Note that D_2 is now forward biased.

Estimate V_1 , V_2 and V_{out} .*

(c) Assuming "true" $\approx 5V$ and "false" $\approx 0.2V$, make a truth table for this gate and see if you can recognize the logical function it performs.

* Hint: Can D_3 and D_4 conduct appreciable current given your value of V_1 ?

Table 5.1 Table of Laplace Transforms (continued) 

| $f(t)$ | Property | $F(s)$ |
|-----------------------------|-------------------------|--------------------------------------|
| $f(t)$ | Definition | $\int_0^\infty f(t)e^{-st} dt$ |
| $f_1(t) + f_2(t)$ | Linearity | $F_1(s) + F_2(s)$ |
| $Kf(t)$ | Linearity | $KF(s)$ |
| $\frac{df(t)}{dt}$ | Differentiation | $sF(s) - f(0)$ |
| $\frac{d^2f(t)}{dt^2}$ | Differentiation | $s^2F(s) - sf(0) - \frac{df(0)}{dt}$ |
| $\int_0^t f(\tau) d\tau$ | Integration | $\frac{1}{s} F(s)$ |
| $tf(t)$ | Complex differentiation | $-\frac{dF(s)}{ds}$ |
| $e^{-at}f(t)$ | Complex translation | $F(s + a)$ |
| $f(t - a)u(t - a)$ | Real translation | $e^{-as}F(s)$ |
| $u(t)$ | | $\frac{1}{s}$ |
| $e^{-at}u(t)$ | | $\frac{1}{s + a}$ |
| $\cos \beta t u(t)$ | | $\frac{s}{s^2 + \beta^2}$ |
| $\sin \beta t u(t)$ | | $\frac{\beta}{s^2 + \beta^2}$ |
| $e^{-at} \cos \beta t u(t)$ | | $\frac{s + a}{(s + a)^2 + \beta^2}$ |
| $e^{-at} \sin \beta t u(t)$ | | $\frac{\beta}{(s + a)^2 + \beta^2}$ |
| $t u(t)$ | | $\frac{1}{s^2}$ |
| $te^{-at}u(t)$ | | $\frac{1}{(s + a)^2}$ |
| $t^n u(t)$ | | $\frac{n!}{s^{n+1}}$ |
| $(1 - e^{-at})u(t)$ | | $\frac{a}{s(s+a)}$ |
| $\delta(t)$ | | 1 |

$$V_R(t) = RI_R(t) \quad \begin{matrix} \xrightarrow{V_R} \\ \text{---} \\ \xrightarrow{I_R} \end{matrix}$$

$$V_C(t) = \frac{1}{C} \int_0^t I_C(t') dt' + \frac{V_C(0)}{C} \quad \begin{matrix} \xrightarrow{V_C} \\ \text{---} \\ \xrightarrow{I_C} \end{matrix}$$

$$V_L(t) = L \frac{d}{dt} I_L(t) \quad \begin{matrix} \xrightarrow{V_L} \\ \text{---} \\ \xrightarrow{I_L} \end{matrix}$$

$$\hat{V}_R(s) = R \hat{I}_R(s)$$

$$* \hat{V}_C(s) = \frac{1}{sC} \hat{I}_C(s)$$

$$** \hat{V}_L(s) = sL \hat{I}_L(s)$$

Note: These require $V_C = 0$ for $t < 0$ (*)
 $I_L = 0$ for $t < 0$ (**)

SOLUTIONS!

16

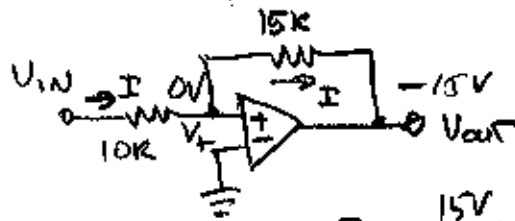
(a) If $V_{in} = -15V$ and $V_{out} = +15V$,

$$V_+ = -15V + \frac{10k}{10k+15k} \times 30V = -3V < V_- = 0V$$

contradiction $\Rightarrow V_{out} = -15V$.

$$\therefore V_+ = -15V$$

(b) Threshold when $V_+ = 0V$, $V_{out} = -15V$.

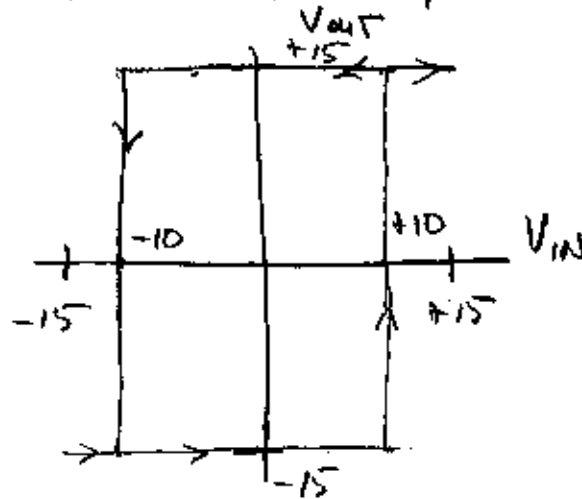


$$I = \frac{15V}{15k\Omega} = 1\mu A$$

$$\therefore V_{in} = +1\mu A \times 10k\Omega = 10V$$

(c) When the threshold is crossed, V_{out} increases toward $+15V$. But this increases V_+ through the $15k$ feedback resistor, making the output increase all the more. \Rightarrow positive feedback.

(d)



Hysteresis: threshold for +ve transition is greater than threshold for -ve transition, leading to a two-valued transfer function between $-10V$ and $+10V$ for V_{in} .

20

$$2(a) H(s) = \frac{R}{R + \frac{1}{sC}} = \frac{s}{s + \frac{1}{RC}} = \frac{s}{s + a}, \quad a = \frac{1}{RC}$$

$$(b) \text{ From table, } \hat{V}_{IN}(s) = \frac{V_0 a}{s(s+a)}$$

$$(c) \hat{V}_{OUT}(s) = H(s) V_{IN}(s) = \frac{V_0 a}{s(s+a)^2} = \frac{V_0 a}{(s+a)^2}$$

$$(d) V_{OUT}(t) = V_0 a t e^{-at} u(t) \\ = \frac{V_0 t}{RC} e^{-t/RC} u(t)$$

15

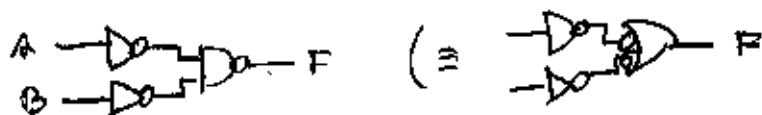
$$3(a) F = \overline{A \oplus B} \cdot \overline{AB}$$

$$(b) = A \oplus B + AB \quad (\text{de Morgan})$$

$$= A\bar{B} + \bar{A}B + AB = A\bar{B} + \bar{A}B + AB + AB$$

$$= A(B + \bar{B}) + (\bar{A} + A)B = \underline{A + B} \quad (\text{or could recognize immediately that } A \oplus B + AB = A + B)$$

$$(c) A + B = \overline{\bar{A}\bar{B}}$$



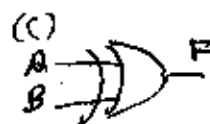
(d) Yes, use two nands as inverters $\neg \neg A = A$ so 3 of the 4 gates are used.

15

4. (a)

| | | | |
|---|---|----|----|
| | | B | |
| | | 00 | 01 |
| A | 0 | 0 | 1 |
| | | 11 | 10 |
| A | 1 | 1 | 0 |

$$(b) F = \bar{A}C + A\bar{C} = A \oplus C$$

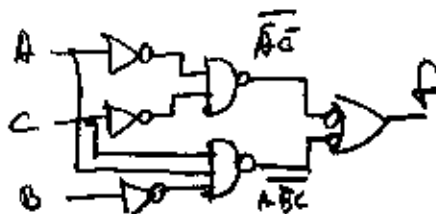


10

5. (a)

| | | | |
|---|---|----|----|
| | | BC | |
| | | 00 | 01 |
| A | 0 | 1 | 0 |
| | | 11 | 10 |
| A | 1 | 0 | 1 |

$$F = \bar{A}\bar{C} + A\bar{B}C$$



20

(a) Q_1 is saturated so $V_{BE} = 0.8V$, $V_{CE} = 0.2V$
 $V_2 = V_{BE} = 0.8V$, $V_{out} = V_{CE} = 0.2V$.

(b) D_2 is forward biased so $V_1 = 0.7V + 0.2V = 0.9V$
At least $1.0V$ would be required for significant current to flow through R_2 in parallel with the BE diode. Thus $V_2 = 0V$ and Q_2 is cut off so $V_{out} = 5V$.

(c)

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$$F = \overline{AB} \text{ (NAND)}$$