Physics 116B Winter 2005: Exam 1

2/4/2005

Closed book and notes except for one $8.5 \text{ in} \times 11 \text{ in}$ sheet of paper. Show reasoning for full credit. There are 4 problems and 100 points (*approximate point values are given*). Note: complex quantities are shown in **boldface** type. All transistors and diodes (if any) are silicon at room temperature unless otherwise noted.

1. (*44 points*) The circuit below shows a TLC555 timer connected as a "one-shot" circuit. The block diagram of the TLC555 (inside the dashed lines) has been simplified slightly for clarity. R and C are connected externally as shown. Initially, $V_{\text{out}}(= Q)$ is low, V_{in} is low and the voltage across the capacitor, $V_C = 0$. Assume the logic levels are 0 and 5 V, the MOSFET has $V_T = 1$ V, $R = 10$ kΩ and $C = 0.01$ μF. Assume that the MOSFET acts like a switch which is open if $V_{GS} < V_T$ and closed for V_{GS} significantly above V_T. See Table 1 for the latch truth table.

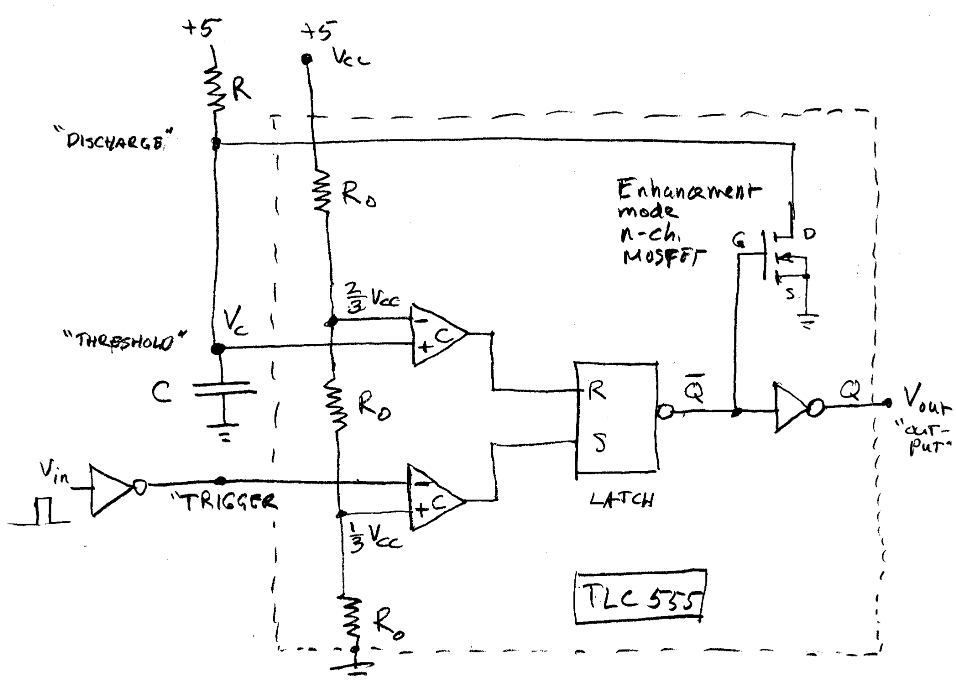
   (a) Explain why $V_C = 0$ given the initial state described above.

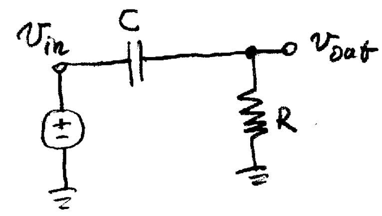
   (b) What are the initial logic levels of "Trigger," R and S? Explain briefly. (R and S are the latch inputs.)

   (c) A 10 μs wide logic pulse is input at V_{in}. Make a timing diagram (3 plots, each stacked above the other, on the same t axis) showing V_{in}, Q and V_{C} during the production of the output pulse *(neglect the internal delays due to the inverter, comparator and latch circuits)*. Explain what causes the latch to be set and what causes it to be reset.

   (d) Write an expression for $V_C(t)$ while Q is high. Use this to find an expression for the width of the output pulse in terms of R and C. Evaluate.

   (e) What happens to V_C when the latch is reset?





2. (*28 points*) In the network above, the voltages and currents are zero for $t < 0$. The input pulse is $v_{\rm in}(t) = kt\ u(t)$, a ramp of slope k V/s starting at $t = 0$. Use the attached Laplace transform table as required for the following. *Note: some additional transform pairs have been added to reduce the need for use of partial fractions.*

   (a) Find $\mathbf{H(s)} \equiv \mathbf{V}_{\rm out}(\mathbf{s})/\mathbf{V}_{\rm in}(\mathbf{s})$ for the circuit.

   (b) Find the Laplace transform of the input waveform and use $\mathbf{H(s)}$ to find $\mathbf{V}_{\rm out}(\mathbf{s})$.

   (c) Find $v_{\rm out}(t)$.

   (d) Make a sketch of $v_{\rm out}(t)$. Does the function have a simple asymptotic form for $t >> RC$?

3. (*10 points*) Use theorems of Boolean algebra to simplify the following logical function:

$$\overline{(A\bar{B} + \bar{A}B)\overline{(AB)}}$$

4. (*18 points*)

   (a) Express the function $F(A, B, C, D)$ given in the Karnaugh map below as a simplified sum of products.

   (b) Implement the function F using two-stage logic with two- and three-input NAND gates and inverters (or even 4-input NANDs if really needed). Remember that De Morgan says that a NAND is equivalent to an OR with inverted inputs.

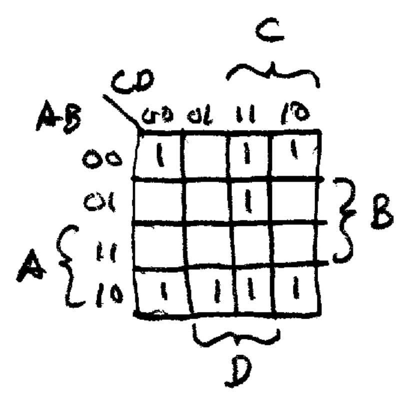


Table 5.1 Table of Laplace Transforms

$f(t)$	Property	$\mathbf{F}(s)$
$f(t)$	Definition	$\int_0^\infty f(t)e^{-st}\,dt$
$f_1(t) + f_2(t)$	Linearity	$\mathbf{F}_1(s) + \mathbf{F}_2(s)$
$Kf(t)$	Linearity	$K\mathbf{F}(s)$
$\frac{df(t)}{dt}$	Differentiation	$s\mathbf{F}(s) - f(0)$
$\frac{d^2f(t)}{dt^2}$	Differentiation	$s^2\mathbf{F}(s) - sf(0) - \frac{df(0)}{dt}$
$\int_0^t f(t)\,dt$	Integration	$\frac{1}{s}\mathbf{F}(s)$
$tf(t)$	Complex differentiation	$-\frac{d\mathbf{F}(s)}{ds}$
$e^{-at}f(t)$	Complex translation	$\mathbf{F}(s + a)$
$f(t - a)\,u(t - a)$	Real translation	$e^{-as}\mathbf{F}(s)$
$u(t)$		$\frac{1}{s}$
$e^{-at}u(t)$		$\frac{1}{s + a}$
$\cos \beta t\, u(t)$		$\frac{s}{s^2 + \beta^2}$
$\sin \beta t\, u(t)$		$\frac{\beta}{s^2 + \beta^2}$
$e^{-\alpha t}\cos \beta t\, u(t)$		$\frac{s + \alpha}{(s + \alpha)^2 + \beta^2}$
$e^{-\alpha t}\sin \beta t\, u(t)$		$\frac{\beta}{(s + \alpha)^2 + \beta^2}$
$t\,u(t)$		$\frac{1}{s^2}$
$te^{-at}u(t)$		$\frac{1}{(s + a)^2}$
$t^n\,u(t)$		$\frac{n!}{s^{n+1}}$
$(1 - e^{-at})\,u(t)$		$\frac{a}{s(s+a)}$
$\delta(t)$		1

Table 1: SR Latch Truth Table (S overrides R)

S	R	Q_n	$Q_\mathrm{n+1}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Q_n is the present state, $Q_\mathrm{n+1}$ is the next state after receiving these inputs.

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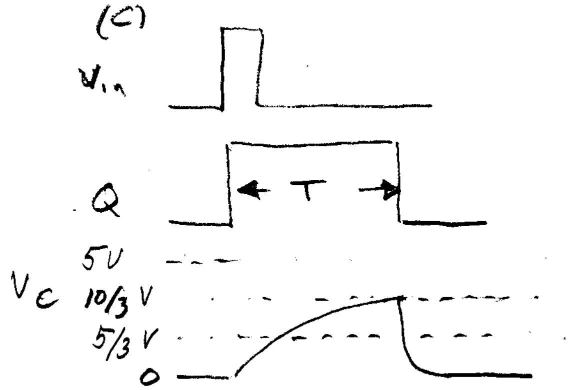
1. (a) $Q=0 \Rightarrow \bar{Q}=1$ and G of MOSFET is at +5 $\Rightarrow$ MOSFET "ON" ($V_{GS}=5V>V_T$) ("closed switch") so "DISCHARGE" is connected to ground, $V_c=0$.

(b) V_{in} = low (0V) so Trigger = 1 so "−" input of S comparator is at $5V > 5/3$ of "+" input so $S=0$.

$V_c=0$ so "+" input of R comparator is less than "−" input $(\frac{2}{3}\times 5V) \Rightarrow R=0$.

(c)



When $V_{in}\to 5V$, Trigger $\Rightarrow 0V < V_+$ on S comparator, $S\to 1$ which causes $Q\to 1$, $\bar{Q}\to 0$. $\bar{Q}\to 0$ turns off MOSFET so capacitor charges toward 5V through R.
When V_c reaches $\frac{10}{3}V$, $R\to 1$, latch resets, $Q\to 0$, $\bar{Q}\to 1$ and V_c falls to 0. [We assume the input pulse is shorter than the time Q is high. Check this next]

(d) While Q is high,

$$V_c = 5V(1-e^{-t/\tau}) \quad \text{where } \tau = RC$$

$$\frac{2}{3}\times \cancel{5V} = \cancel{5V}(1-e^{-T/\tau}) \Rightarrow e^{-T/\tau}=\frac{1}{3}$$

$$e^{T/\tau}=3 \Rightarrow T=\tau\ln 3 = 10000\times .01\times 10^{-6}\times 1.1\,s$$

$$= 1.1\times 10^{-4}s = 110\,\mu s \quad (\gg 10\,\mu s)$$

(e) When the latch is reset, the MOSFET is turned on, causing $V_c \to 0$.

28 2.

(a) $$\underset{\sim}{H}(s) = \frac{v_{out}}{v_{in}} = \frac{R}{R + \frac{1}{sC}} = \frac{s}{s + \frac{1}{RC}}$$

(b) $V_{in}(t) = k\,t\,u(t) \Rightarrow \underset{\sim}{V}_{in}(s) = \underline{k/s^2}$

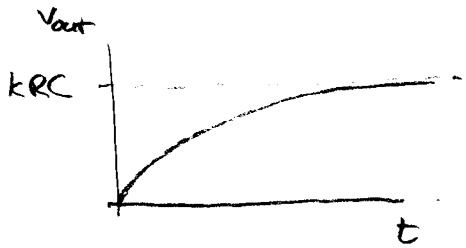
$$\underset{\sim}{V}_{out}(s) = \underset{\sim}{H}\,\underset{\sim}{v}_{in} = \frac{k}{s^2}\,\frac{s}{s + \frac{1}{RC}} = \underline{\frac{k}{s(s + \frac{1}{RC})}}$$

(c) $V_{out}(s) = \frac{k}{a}\,\frac{a}{s(s+a)}$ where $a = \frac{1}{RC}$

$$V_{out}(t) = \frac{k}{a}\left(1 - e^{-at}\right)u(t)$$

$$= \underline{\underline{kRC\left(1 - e^{-t/RC}\right)u(t)}}$$

(d)



yes, $V_{out} \to kRC$

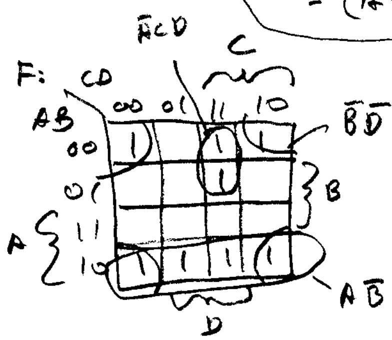
$\left(V_{out} \to RC\,\frac{dV_{in}}{dt}\right)$

10 3. $$\overline{(A\bar{B} + \bar{A}B)(\overline{AB})} = A\bar{B} + \bar{A}B + AB \quad \text{(De Morgan)}$$

$$= A\bar{B} + (\bar{A}+A)B = A\bar{B} + B$$

$$= (A+B)(\bar{B}+B) = \underline{A+B}$$

18 4.



$\bar{B}\bar{D}$ (all four corners are 1)

$F = A\bar{B} + \bar{A}CD + \bar{B}\bar{D}$