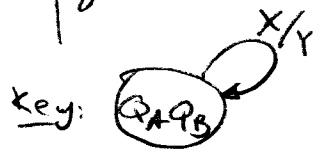


35

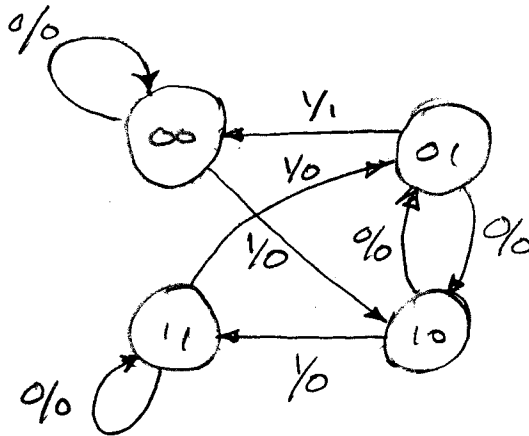
1.

(a)

X	Q _A	Q _B	X ⊕ Q _B = Q _A (t+1)	Q _A = Q _B (t+1)	X̄Q _A Q _B = Y
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0



(b)



(c) Min. period = Max. FF delay + Max. XOR delay + Min. Setup t
 = 30 ns + 18 ns + 25 ns = 73 ns

Max. Frequency = 1 / min. period = 1 / 73 ns = 13.7 MHz

(d) 00 → 01 → 10 → 11 → 00 etc. This is counting backward in Gray code.

(e) The X input could cause Q_A to change within the setup time prior to and the hold time just after the clock pulse when the input should be stable. This could lead to metastability in the A flip-flop (it could get "stuck" in some improper state for an unknown length of time). A remedy is to include one or more D flip-flops synchronized with the system clock between X and the XOR input node:



35 2. (a) leading edge triggered

(b)

Transition map: FF2

$\alpha=0 \Rightarrow 1$ $\beta=1 \Rightarrow 0$
 $0=0 \Rightarrow 0$ $1=1 \Rightarrow 1$

FF2:

	Q_1, Q_2			
X	00	01	11	10
0	α	1	β	α
1	0	1	β	α

J_2 :

	Q_1, Q_2			
X	00	01	11	10
0	1	X	X	1
$X \sum 1$		X	X	1

$$J_2 = \bar{X} + Q_1$$

$$(\quad = \overline{X \bar{Q}_1})$$

K_2 :

	Q_1, Q_2			
X	00	01	11	10
0	X		1	X
$X \sum 1$	X		1	X

$$K_2 = Q_1$$

(c) Y :

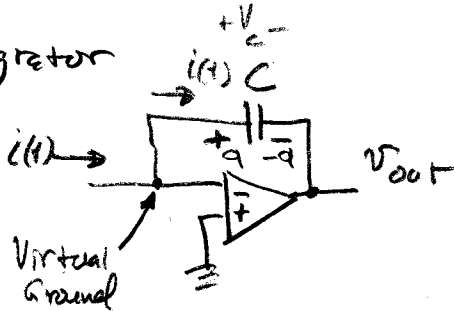
	Q_1, Q_2			
X	00	01	11	10
0	1		1	
$X \sum 1$		1		

$$Y = \bar{X} \bar{Q}_1 \bar{Q}_2 + \bar{X} Q_1 Q_2 + X \bar{Q}_1 Q_2$$

(K. map no help)

30 3. (b) i.) integrator

ii.)



$$V_c = 0 \text{ at } t = 0$$

$$\frac{dq}{dt} = i = C \frac{dV_c}{dt}$$

$$\frac{dq}{dt} = -C \frac{dv_{out}}{dt}$$

$$Q = \int_{t_1}^{t_2} \frac{dq}{dt'} dt'$$

$$= -C \int_{t_1}^{t_2} \frac{dv_{out}}{dt'} dt'$$

$$= -C v_{out}(t_2)$$

$$v_{out}(t_2) = -Q/C$$

(polarity is neg.)

iii) Yes since charge remains on C, $i(t) = 0$
since i into $-$ input of op-amp ≈ 0 .

iv) $-$ input $<$ $+$ input so G is high

(c) i.) Now $i(t) = -V_{REF}/R = -C \frac{dv_{out}}{dt}$

$$\frac{dv_{out}}{dt} = + \frac{V_{REF}}{RC}$$

$$ii) t = \left| \frac{v_{out}(t_2)}{\frac{dv_{out}}{dt}} \right| = \frac{Q RC}{V_{REF}} = \frac{QR}{V_{REF}}$$

iii) When v_{out} slightly exceeds 0V, G goes low and the clock pulse to the counter is gated off. The clock had been gated on when W went high (with the counter reset) when switch Y was closed allowing the capacitor to start charging. Thus the number of counts = $t/\text{clock period}$

$$iv) N = t/T = \frac{QR}{V_{REF} T} = \frac{QR}{V_{REF}} f \propto Q$$

($T \equiv$ clock period)