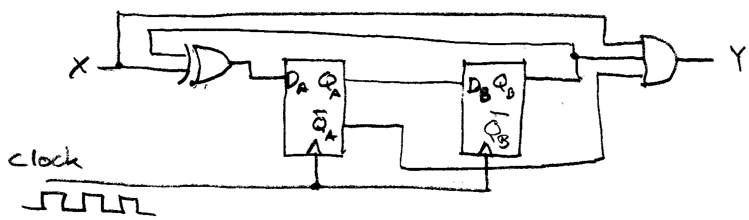
# Physics 116B Winter 2004: Exam 2

3/3/2004

Closed book and notes except for two $8.5\ \mathrm{in} \times 11\ \mathrm{in}$ sheets of paper. Show reasoning for full credit. There are 3 problems and 100 points.




1. (a) Make a complete state table for the synchronous sequential circuit above. Note that there is one input and one output.

   (b) Determine the complete state diagram for the circuit. Label the transitions with the values of the input and output using the notations, 0/0, 0/1, 1/0 or 1/1, as appropriate.

   (c) Calculate the maximum clock frequency for the circuit using the specifications in Table 1.

   (d) If the input $X$ is held at logical 1 continuously, does the circuit execute the same sequence of states, no matter which state it starts in? If so, do you recognize the sequence?

   (e) Assume that the $X$ input is not synchronized with the clock. Can this cause a problem for the circuit? Explain and, if possible, suggest additional circuitry to remedy this condition (without adding more external inputs or outputs).

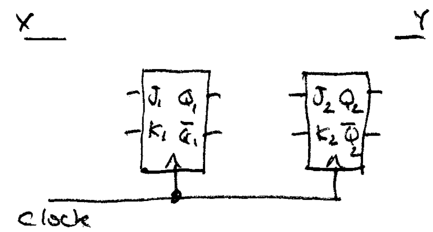
Table 1: Chip Timing Specifications for Problem 1

| **Parameter** | **Maximum** | **Typical** | **Minimum** |
|---|---|---|---|
| AND propagation delay | 12 ns | 8 ns | - |
| XOR propagation delay | 18 ns | 12 ns | - |
| Filp-flop propagation delay | 30 ns | 20 ns | - |
| Filp-flop setup time | - | - | 25 ns |
| Filp-flop hold time | - | - | 5 ns |
| Filp-flop clock pulse width | - | - | 20 ns |
| Filp-flop clock frequency | 30 MHz | - | - |

State Table for Problem 2

| $X$ | $Q_1$ | $Q_2$ | $Q_1(t+1)$ | $Q_2(t+1)$ | $Y$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

Skeleton Circuit:




2. (a) The flip-flops above are (chose one) (leading edge triggered; trailing edge triggered; pulse-triggered master-slave).

   (b) For the state table above, find the logical functions required for $J_2$ and $K_2$ in simplified sum-of-products form. You do not need to draw the circuits–just find the necessary input logical functions. (Also, you don't need to do flip-flop 1 inputs.)

   (c) Find the function for the output, Y, in simplified sum-of-products form.

For reference, here are the input equations for the JK flip-flop:

Input equations for JK flip-flop:

$J = \alpha$ (transitions where J must equal 1)
$DC_J = \beta, 1, X$ (transitions for which we don't care what J is)
$J = 0$ otherwise.

$K = \beta$ (similarly for K)
$DC_K = \alpha, 0, X$

3. The circuit on the next page represents a charge digitizer. The logic signals and basic operation of the circuit are also explained there. *Note: This is a simple circuit to demonstrate the principle of operation. Improvements in the control circuitry could be added to make the digitizer operation more efficient.*

   (a) *Reset:* First, the circuit is reset so $v_{\mathrm{out}} = 0$ and the counter data, N=0. W is low so the counter is not counting.

   (b) *Sample and Hold:* At time $t_1$, ACQUIRE goes high, closing switch X and allowing current $i(t)$ to flow into the op-amp circuit. ACQUIRE goes low at $t_2$. Let $Q$ be the total charge flowing into the circuit during the time interval while ACQUIRE is high. Clearly, $Q = \int_{t_1}^{t_2} i(t)\,\mathrm{d}t$.

      i. The op-amp circuit performs a mathematical operation on the input current. It is (choose one) (a current to voltage converter; a summing amplifier; a differentiator; an integrator or: none of the above).

      ii. Find an expression for $v_{\mathrm{out}}(t_2)$ in terms of $Q$ and C. What is the polarity of this voltage, given that $Q > 0$.

      iii. Will $v_{\mathrm{out}}$ remain constant (approximately) if switches X, Y and Z remain open?

      iv. Find the logic level at the comparator output at time $t_2$.

   (c) *Digitize:* The DIGITIZE signal is now held high for the length of time required for the counter to count 255 clock pulses. The switch Y is closed and W is high while DIGITIZE is high. This connects the inverting input of the op-amp to $-V_{\mathrm{ref}}$ through the resistor, R. W is one of the signals controlling the clock input to the counter.

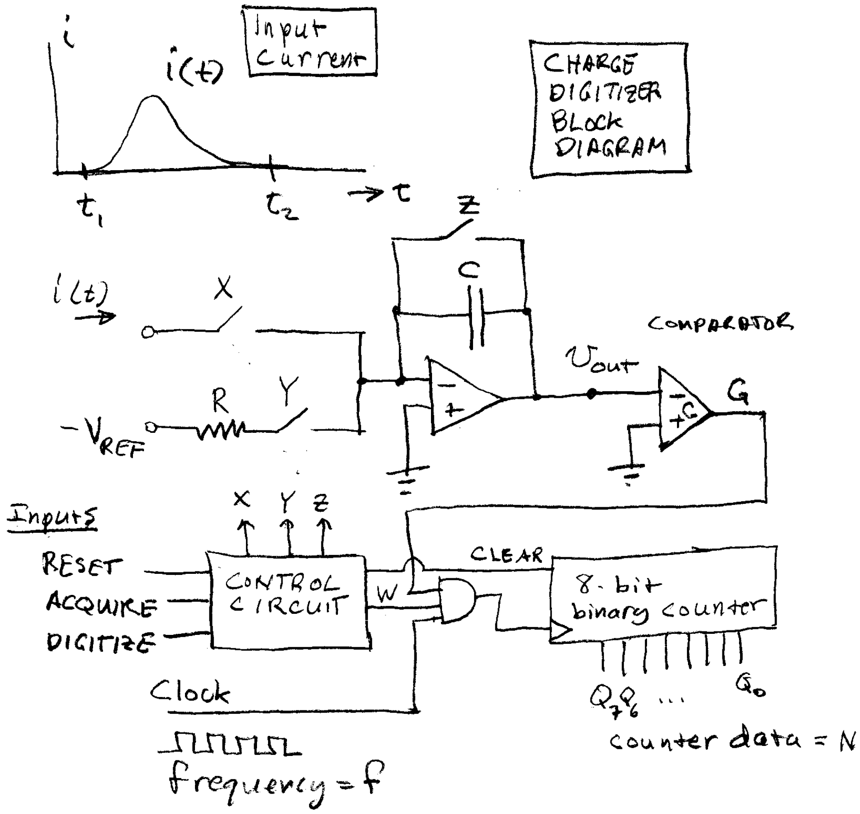
      i. Find $\frac{dv_{\mathrm{out}}}{dt}$ in terms of $V_{\mathrm{ref}}$, C and R while DIGITIZE is high.

      ii. Find the length of time required for $v_{\mathrm{out}}$ to reach 0. Express your result in terms of $V_{\mathrm{ref}}$, $Q$, C and R.

      iii. Assume that this time is less than the time for the counter to reach full scale. Explain why the counter stops counting and contains a number $N$ proportional to $Q$.

      iv. Find an expression for $N$ in terms of the clock frequency, $f$, $V_{\mathrm{ref}}$, $Q$, R and C.

Figure for Problem 3:




Operation: • The control circuit outputs are X, Y, Z, W, and CLEAR.

• X, Y and Z are normally open, W and CLEAR are normally low (false).

• A high level on RESET causes switch Z to close and the CLEAR signal to be high, discharging C and resetting the counter.

• A high level on ACQUIRE causes X to close.

• A high level on DIGITIZE causes W to go high for a time sufficient for the counter to reach its maximum value, at the same time closing Y for this time interval.