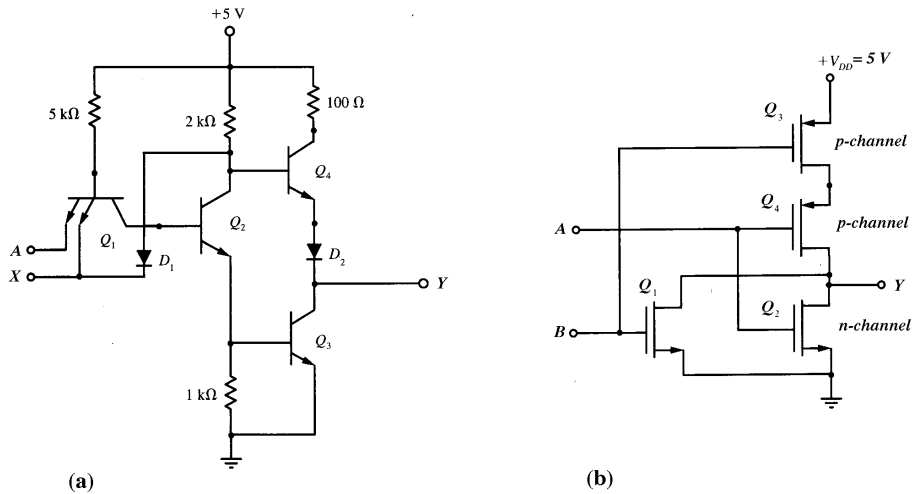


Physics 116B Winter 2005: Exam 2

3/2/2005

Closed book and notes except for two 8.5 in \times 11 in sheets of paper. Show reasoning for full credit.

There are 3 problems and 100 points.



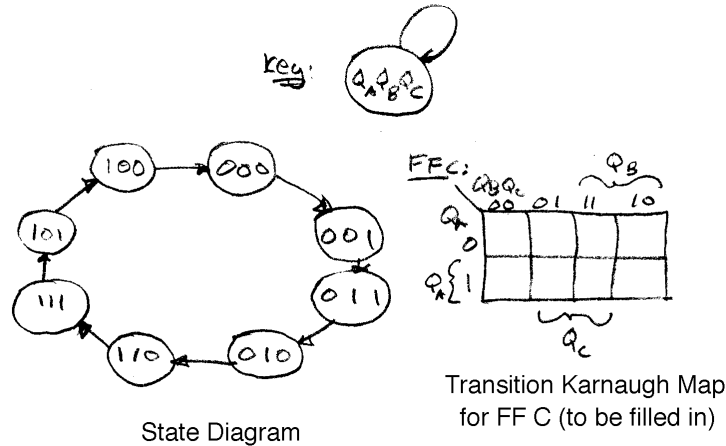
1. (≈ 40 points) In these diagrams, crossing wires with no dot do not connect.

(a) First, consider the logic circuit in Fig. (a), above.

- i. Suppose both X and A are at 5 V. What are the states of Q_2 , Q_3 and Q_4 (on or off)? What is the state of the output (H, L, high-Z)? Explain briefly. (Note that when X is at 5 V, D_1 is not forward biased so \approx no current flows through it).
- ii. Now suppose X is at 5 V and A is at 0 V. What are the states of Q_2 , Q_3 and Q_4 (on or off)? What is the state of the output (H, L, high-Z)? Explain briefly.
- iii. Finally, suppose X is at 0 V and A is at 0 V. What are the states of Q_2 , Q_3 and Q_4 (on or off)? What is the state of the output (H, L, high-Z)? Explain briefly.
- iv. When X is at 5 V, what logic function of A does the gate provide?
- v. Explain briefly why the X input could be useful for something.
- vi. What would be the advantage for the circuit if the transistors were replaced with Schottky transistors? (Recall that a Schottky transistor has a Schottky diode connected between the base and the collector.)

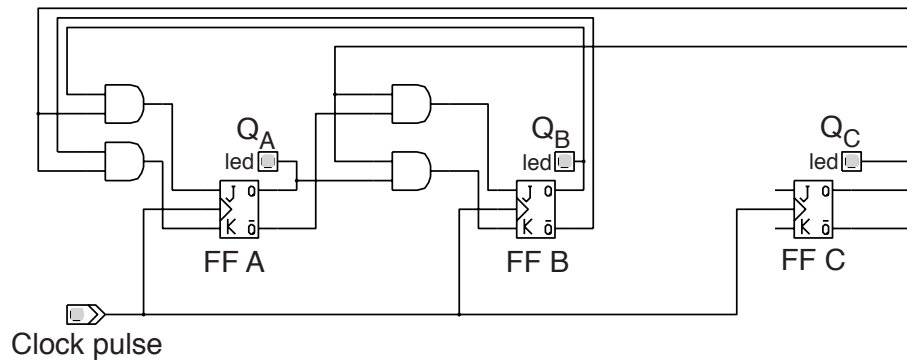
(b) Now consider circuit (b). Assume the logic levels are H = 5 V and L = 0 V.

- i. Suppose A and B are both H. Find V_{GS} for Q_1 and Q_3 and state whether the MOSFET is on or off. Use this information to find the output voltage at Y .
- ii. For what combinations of the input states will the output be high? Explain briefly.
- iii. What is the logic function performed by the circuit?
- iv. Why could damage occur to the circuit if B is low and A is left floating (i.e., not connected to a valid logic level)?



2. (≈ 36 points) We wish to design a Gray code counter using JK flip-flops (FF). The state diagram is shown above. A partial circuit design is shown below. (Lines crossing at right angles don't connect.) Only FF C remains to be done. An empty transition Karnaugh map is given (to be filled with α , β , 0, 1 and x, as usual).

- The flip-flops below are (choose one): (leading edge triggered; trailing edge triggered; master-slave).
- The circuit shown is (choose one): (synchronous; asynchronous). Explain briefly.
- Make the transition Karnaugh map for FF C. From it, make the Karnaugh maps for the J_C and K_C inputs. (Note: the input equations for the JK flip-flop are given on the next page. You may also use the text method without the transition map at your own risk).
- Design the logic circuits to connect to J_C and K_C . You may use ANDs, ORs, Exclusive ORs, and inverters. Be efficient in the use of gates, avoiding unnecessary delays. You may label the input and output lines on your diagrams with the logical variable names to avoid redrawing the entire circuit.
- Calculate the maximum clock frequency for the circuit using the specifications in Table 1. Note: If you do not finish your design, just find the maximum clock frequency for the circuit as given without considering the inputs of FF C.



Information for Problem 2:

Input equations for JK flip-flop:

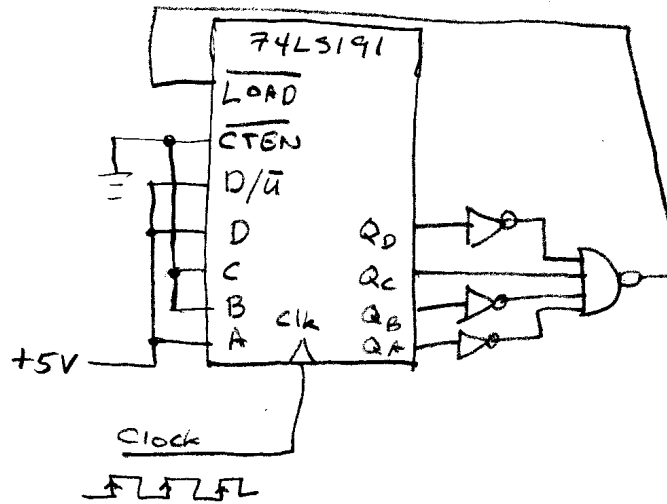
$$\left\{ \begin{array}{l} J = \alpha \quad (\text{transitions where } J \text{ must equal } 1) \\ DC_J = \beta, 1, x \quad (\text{transitions for which we don't care} \\ \quad \text{what } J \text{ is}) \\ J = 0 \text{ otherwise.} \end{array} \right.$$

$$\left\{ \begin{array}{l} K = \beta \quad (\text{similarly for } K) \\ DC_K = \alpha, 0, x \end{array} \right.$$

Table 1: Chip Timing Specifications for Problem 2

Parameter	Maximum	Typical	Minimum
AND propagation delay	12 ns	8 ns	-
OR propagation delay	12 ns	8 ns	-
INVERTER propagation delay	10 ns	7 ns	-
XOR propagation delay	18 ns	12 ns	-
Flip-flop propagation delay	30 ns	20 ns	-
Flip-flop setup time	-	-	25 ns
Flip-flop hold time	-	-	5 ns
Flip-flop clock pulse width	-	-	20 ns
Flip-flop clock frequency	30 MHz	-	-

(Go on to Problem 3)



3. (≈ 24 points) The circuit above is made with a 74LS191 synchronous binary up/down counter with asynchronous load. Specifications for the counter are attached. After the clock is started, the counter eventually enters a repetitive sequence of states.
- Make a complete state diagram showing the repetitive sequence. Label each state with the decimal number corresponding to the state (Q_A is the least significant bit). Indicate any transitions which are not synchronous with the clock.
 - Assume the clock period is much longer than the time for the asynchronous transition. What is the sequence of states observed immediately prior to the clock transitions?
 - In this sequence, are there any transitions which could produce glitches on the $\overline{\text{LOAD}}$ input? If so, which ones? What sort of problem could this cause for the circuit?

1. (a) i) Q_2 ON, Q_3 ON, Q_4 OFF. $\Rightarrow Y$ is L.

With A, X both high, Q_1 is in reverse active mode which pulls the base of Q_2 up, turning it on.

This pulls up the base of $Q_3 \Rightarrow Q_3$ on, pulls down the base of Q_4 . Detailed calculation shows V_{BE} of Q_4 below 0.5V so Q_4 off.

ii) With A at 0V, Q_1 is on, pulling base of Q_2 toward ground and turning Q_2 off. With Q_2 off, base of Q_3 is $\approx 0V \Rightarrow$ Q_3 off. Base of Q_4 is pulled up through 2k Ω resistor to +5V so Q_4 is on. With Q_4 on, Q_3 off, Y is H.

iii) This is like ii) except X is also low. This means Q_1 must be ON (X low would guarantee this independent of A). But since X=0V, the base of Q_4 is one forward diode drop above ground so Q_4 is off. Since Q_2 is off, Q_3 is off. The output is in the High-Z state.

iv) $X = 5V \Rightarrow$

A	Y
H	L
L	H

 \Rightarrow inverter. $Y = \bar{A}$

v) When X is low the output is in the high-Z state. X serves as an "output enable" input, useful for connecting the output to a shared data line.

vi) Schottky transistors prevent the BJTs from being saturated, ensuring faster turn-off. Thus circuits can be produced with shorter gate delays.

(b) i) $A = B = 5V$

For Q_1 $V_{GS} = V_G - U_S = 5V - 0V = 5V \Rightarrow Q_1$ ON

For Q_3 $V_{GS} = 5V - 5V = 0V \Rightarrow Q_3$ OFF

Since Q_1 ON, Q_3 OFF, $Y = 0V$.

ii) For the output to be high, Q_1 and Q_2 must be off and Q_3 and Q_4 must be on. This is the case if and only if A and B are low.

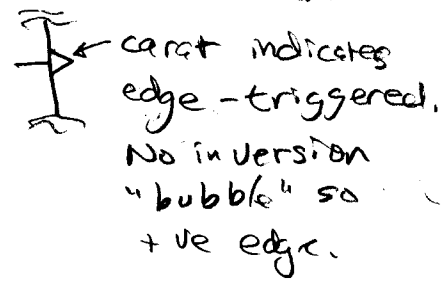
iii) $Y = \overline{AB} = \overline{(A+B)}$ ("nor" circuit)

iv) If B is low, Q_3 is on and Q_1 is off.

Now if A is floating, it could go to $V \approx 2.5V$ where Q_3 and Q_4 are on.

Thus, there would be a path from V_{DD} to ground through the MOSFETs which could lead to excessive power dissipation, burning out the gate.

2. (a) leading edge triggered (as one can tell from the clock input symbol):



(b) Synchronous. All clock inputs respond only to the external clock, not other signals.

(c) FFC:

	Q_B	00	01	11	10
Q_A	0	0	1	0	1
Q_A	1	0	0	1	0

Jc:

	Q_B	00	01	11	10
Q_A	0	1	x	x	
Q_A	1		x	(x)	1

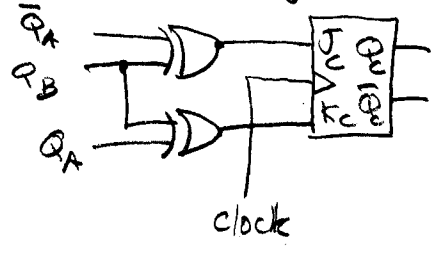
$$J_c = \bar{Q}_A \bar{Q}_B + Q_A Q_B = (\bar{Q}_A) \bar{Q}_B + (Q_A) Q_B = \bar{Q}_A \oplus Q_B (= Q_A \oplus \bar{Q}_B = \overline{Q_A \oplus Q_B})$$

Kc:

	Q_B	00	01	11	10
Q_A	0	x		1	x
Q_A	1	x	1		x

$$K_c = Q_A \bar{Q}_B + \bar{Q}_A Q_B = Q_A \oplus Q_B$$

(d) one solution (min. gate delays).



(e) Max. gate delay = FF delay + exclusive or delay

$$T_{min} = \text{min. setup time} + \text{max. FF delay} + \text{max. XOR delay} = 25 \text{ ns} + 30 \text{ ns} + 18 \text{ ns} = \underline{73 \text{ ns.}}$$

$$f_{max} = 1/T_{min} = \underline{13.7 \text{ MHz}}$$

(without the FF c inputs, substitute AND for XOR, 6 ns less delay $\Rightarrow T_{min} = 67 \text{ ns}$, $f_{max} = \underline{14.9 \text{ MHz}}$)

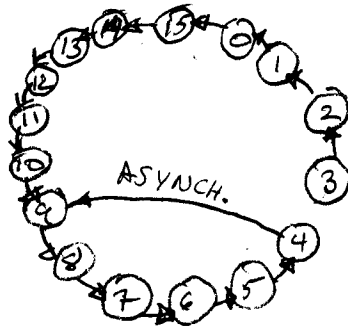
3. (a) The circuit presets asynchronously when

$$Q_D Q_C Q_B Q_A = 0100 \text{ (State 4).}$$

It is preset to state 1001 = 9. (Asynchronous preset)

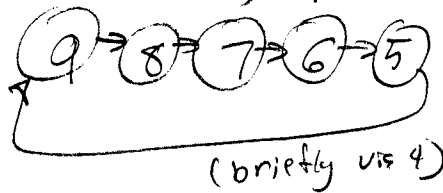
The circuit counts down since $D/\bar{u} = 5V$ and $\overline{CTEN} = 0V$.

State diagram.



(b) ④ is a "transient" state - remains only as long as it takes for the preset to 9 to occur.

If $T \gg$ preset time, apparent sequence is



(c)	9	1001	↓
	8	1000	no
	7	0111	yes
	6	0110	no
	5	0101	yes
	4	0100	-

Can transition momentarily fake 0100 and cause preset? (at least in principle?)

8→7 and 6→5 could have glitches.

In principle, glitch could cause premature presets and occasional incorrect sequences.