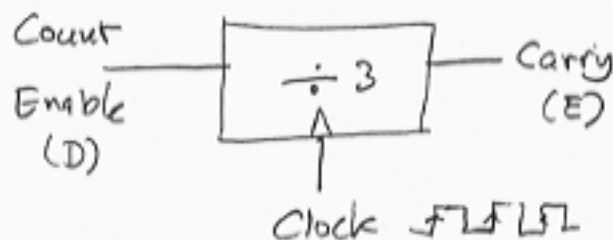


Synchronous Sequential Circuit Design

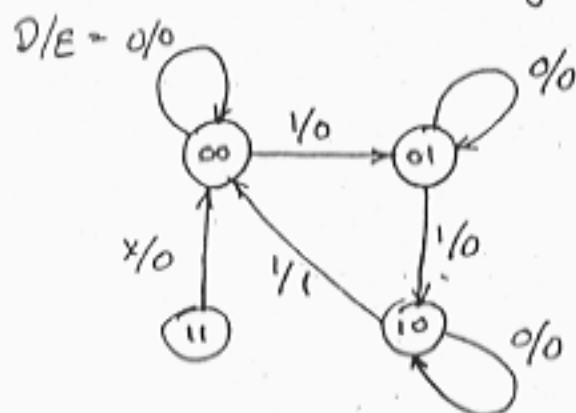
Example: synchronous $\div 3$ counter with "count enable" input and "carry" output.

Use Mealy model: output depends on state & input. The transition diagram is given in the next section.



State assignment (make self-starting):

We wish to implement the following transition diagram using JK flip-flops and gates:

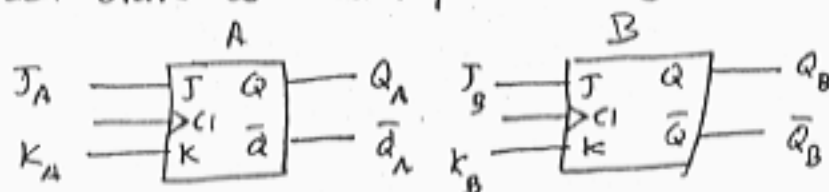


Key: $\textcircled{10}$ = state

\curvearrowright = transition after clock pulse

$1/0$ = input(s)/output(s)

Each state will be represented by two flip-flops, A and B:



Thus, the state 10 is represented by $Q_A = 1, Q_B = 0$.

Let D represent the input signal and E the output.

We now need to figure out how to write functions for $J_A, K_A, J_B, K_B,$ and E as functions of $Q_A, Q_B,$ and $D.$

Step I: make a transition map for each flip-flop which tells what the flip-flop is supposed to do at each transition of the diagram above. The transition map is a Karnaugh map with elements as shown in the table below:

<u>flip-flop transition</u>	<u>element in transition K. map</u>
$1 \rightarrow 1$	1
$0 \rightarrow 0$	0
$0 \rightarrow 1$	α
$1 \rightarrow 0$	β
don't care	x

For example, the transition map for flip-flop A is:

A:

D	$Q_A Q_B$			
	00	01	11	10
0	0	0	β	1
1	0	α	β	β

We fill in the boxes by reading the transitions from the transition diagram.

Similarly, for flip-flop B, we get:

B:

D	$Q_A Q_B$			
	00	01	11	10
0	0	1	β	0
1	α	β	β	0

Step II:

We now translate these transition maps to Karnaugh maps for the flip-flop inputs by using the properties of the flip-flop used. For a JK flip-flop,

J must be 1 for β ,
 We don't care what J is for $\beta, 1, x$,
 and J must be 0 for 0.

K must be 1 for β ,
 we don't care what K is for $\alpha, 0, x$,
 and K must be 0 for 1.

These are summarized in the "input equations" for the flip-flop discussed in Peatman, The Design of Digital Systems, Fig. 5-12.

For a JK flip-flop, we have:

$$\begin{cases} J = \alpha \\ DC_J = \beta, 1, x \end{cases} \begin{cases} (\text{transitions where } J \text{ must equal } 1) \\ (\text{transitions for which we don't care} \\ \text{what } J \text{ is}) \\ (J = 0 \text{ otherwise}) \\ (\text{similarly for } k) \end{cases}$$

$$\begin{cases} K = \beta \\ DC_K = \alpha, 0, x \end{cases}$$

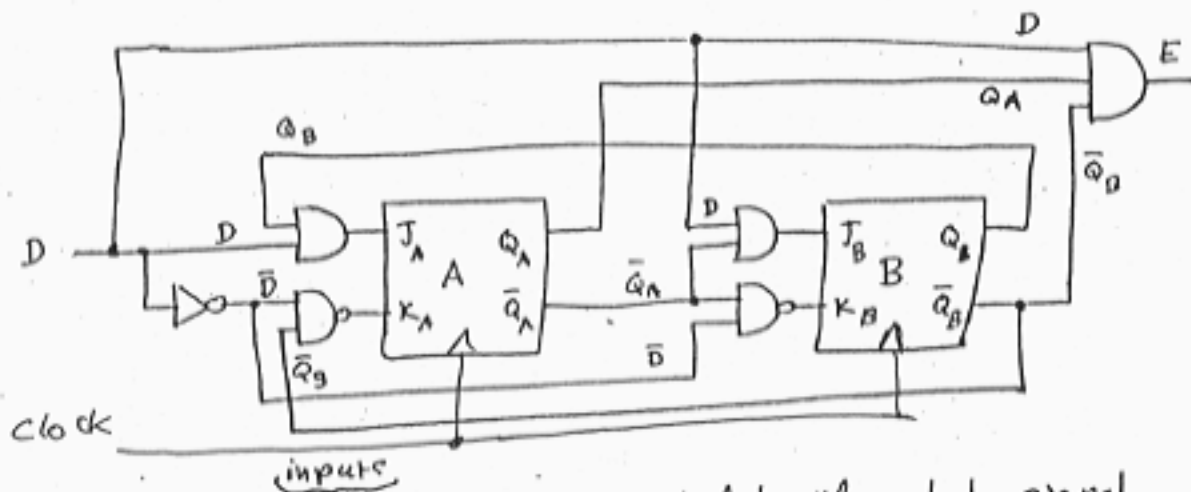
We use these to perform the translation of the transition maps to Karnaugh maps for the four inputs:

$$\begin{array}{l} J_A: \begin{array}{c} Q_A Q_B \\ D \quad 00 \quad 01 \quad 11 \quad 10 \\ 0 \quad 0 \quad 0 \quad X \quad X \\ 1 \quad 0 \quad 1 \quad X \quad X \end{array} \quad J_A = Q_B D \\ \\ K_A: \begin{array}{c} Q_A Q_B \\ D \quad 00 \quad 01 \quad 11 \quad 10 \\ 0 \quad X \quad X \quad 1 \quad 0 \\ 1 \quad X \quad X \quad 1 \quad 1 \end{array} \quad \begin{array}{l} \bar{K}_A = \bar{D} \bar{Q}_B \\ \text{or} \\ K_A = \bar{D} \bar{Q}_B \end{array} \\ \\ J_B: \begin{array}{c} Q_A Q_B \\ D \quad 00 \quad 01 \quad 11 \quad 10 \\ 0 \quad 0 \quad X \quad X \quad 0 \\ 1 \quad 1 \quad X \quad X \quad 0 \end{array} \quad J_B = D \bar{Q}_A \\ \\ K_B: \begin{array}{c} Q_A Q_B \\ D \quad 00 \quad 01 \quad 11 \quad 10 \\ 0 \quad X \quad 0 \quad 1 \quad X \\ 1 \quad X \quad 1 \quad 1 \quad X \end{array} \quad \begin{array}{l} \bar{K}_B = \bar{Q}_A \bar{D} \\ \text{or} \\ K_B = \bar{D} \bar{Q}_A \end{array} \end{array}$$

(Note that it is easier to implement the complement of K_A and K_B , then invert to get the desired fcn.)

Finally, we note $E = D Q_A \bar{Q}_B$.

This is the resulting circuit:



The clock _A are both connected to the clock signal.

This circuit would be called a synchronous, self-starting modulo three counter with carry out port and count enable.

For further study: Figure out the input equations for D or T flip-flops. Design a counter using these instead of JK flip-flops.

Reference: Peatman, The Design of Digital Systems, ch. 5.

Further input equations for D FF:

$$\left. \begin{array}{l} D \text{ must be } 1 \text{ for } \alpha, 1 \\ \text{ " " } 0 \text{ for } \beta, 0 \\ \text{only "don't care" condition is } x \end{array} \right\} \begin{cases} D = \alpha, 1 \text{ (i.e., } \neq \beta \alpha, 1) \\ DC_D = x \\ (D = 0 \text{ otherwise)} \end{cases}$$

$$\left. \begin{array}{l} T \text{ FF: } T \text{ must be } 1 \text{ for } \alpha, \beta \\ \text{ " " } 0 \text{ for } 0, 1 \\ \text{only "don't care" condition is } x \end{array} \right\} \begin{cases} T = \alpha, \beta \text{ (i.e., } T = 1 \text{ for } \alpha, \beta) \\ DC_T = x \\ (T = 0 \text{ otherwise)} \end{cases}$$