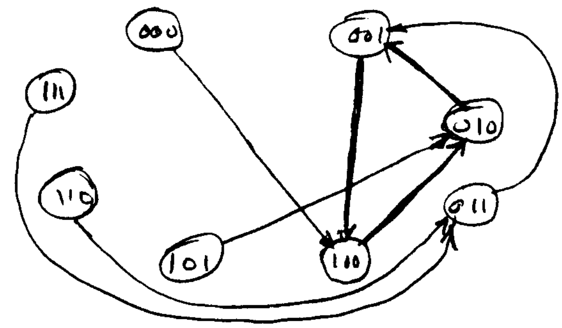
Manuscript problems

1. (a) $D_A = \overline{Q_A + Q_B}$



(b) 

(c) The circuit is synchronous because all flip-flop transistions are synchronized with the clock pulse (i.e, clock inputs connect only to clock signal, not to other signals.)

(d) Minimum period = ff max. delay + NOR max. delay + ff minimum setup time

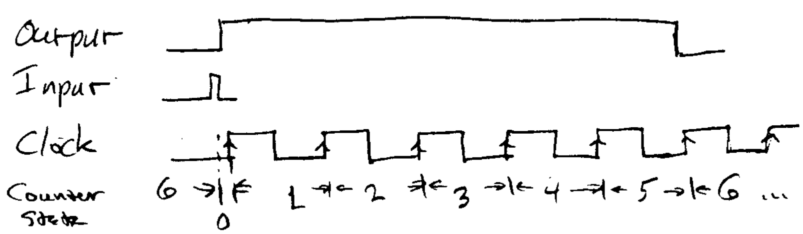
$= 30\,ns + 15\,ns + 25\,ns = 70\,ns$

(note that constrain on min. clock pulse width of 20 ns can be easily satisfied with this period)

$f_{max} = 1/\text{min. period} = \underline{14.3\ MHz}$.

2. (a) The counter is initially 0. It counts up until Q_1 and Q_2 are both 1, at which point the count enable (active low) input goes to 1 and further counting is disabled. Thus, the counter is in the state 0110 = "6" and the output is $\overline{1 \cdot 1} = 0$.

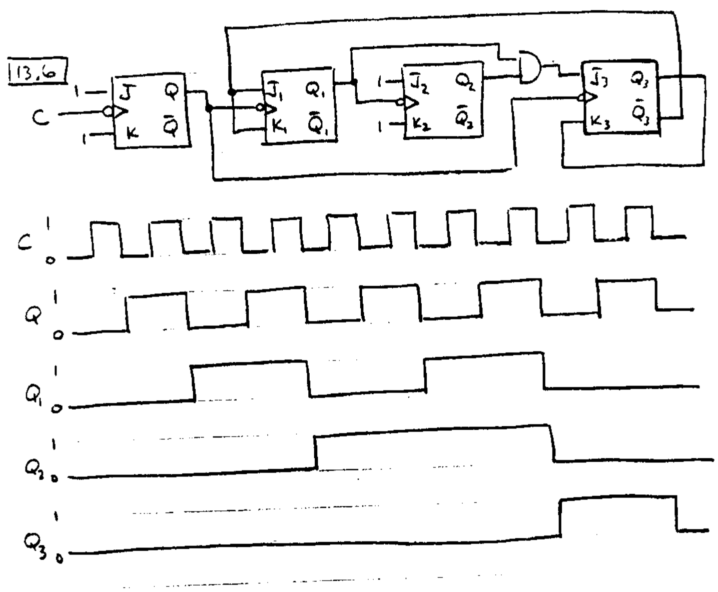
(b) The counter is reset to zero, so $\overline{\text{count enable}} = 0$ and remains 0 at the clock transitions until the state "6" is reached. During this time the output is high. The minimum length of the output pulse is slightly more than 5 clock cycles (the $\overline{\text{clear}}$ input must arrive slightly before the clock transition for an immediate $0 \to 1$ transition of the counter. Then there are 5 full states (1, 2, 3, 4, 5). On the sixth clock edge, the reaches 6, the output goes low, and counting stops.



Min. output pulse width $\approx 5 \times 10\,\mu s = \underline{50\,\mu s}$

(c) The output pulse is extended to $\gtrsim 50\,\mu s$ after the second pulse (second input resets the counter to 0).

(d) Yes - for example, in the transition from 011 to 100, the 110 state can momentarily appear and result in a glitch (toward 0) of the output pulse. (This will not affect the count sequence since the glitch is momentary (!) and does not come during the "setup time" for the clock enable input. A glitch on the clear input is another story).

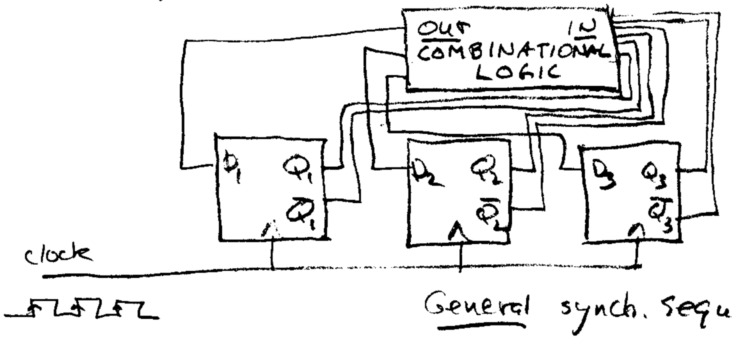


13.35

(d.) $\frac{1}{2^n} = \frac{1}{2^6} = \frac{1}{64} = \underline{\underline{1.56\%}}$

(e) $\frac{1}{2^n} = \frac{1}{2^8} = \frac{1}{256} = \underline{\underline{0.39\%}}$

Problem based on 13.15: Actually, this sequence can't be realized using the circuit of P13.13 (sorry 'bout that!). It can, of course be realized with D ff's and more general feedback logic as follows:



General synch. sequential circuit w/D ff's

State Table

Present State (n)			next state (n+1)		
Q_1	Q_2	Q_3	Q_1	Q_2	Q_3
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

To achieve the next state, $D_{i_n} = Q_{i_{n+1}}$.

We now make K. maps for each D input.

(You could also use the general transition map approach).

D_1:

$Q_1 \backslash Q_2Q_3$	00	01	11	10
0	0	0	0	1
1	0	1	1	1

D_2:

$Q_1 \backslash Q_2Q_3$	00	01	11	10
0	0	1	1	1
1	0	0	0	1

D_3:

$Q_1 \backslash Q_2Q_3$	00	01	11	10
0	1	1	0	0
1	0	0	1	1

$$D_1 = Q_1Q_3 + Q_2\overline{Q}_3$$

$$D_2 = \overline{Q}_1Q_3 + Q_2\overline{Q}_3$$

$$D_3 = \overline{Q}_1\overline{Q}_2 + Q_1Q_2 = (\overline{Q}_1)\overline{Q}_2 + (\overline{\overline{Q}_1})Q_2 = \overline{Q}_1 \oplus Q_2$$

Circuit: