

Physics 116 B Logic Circuit  
Handout problems - solutions

TTL circuit

N = on, F = off

A	B	$I_{CQ1}$	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	Y
0	0	+	F	F	N	F	N	0
0	1	+	F	F	N	F	N	0
1	0	+	F	F	N	F	N	0
1	1	-	N	N	F	N	F	1

} "AND"

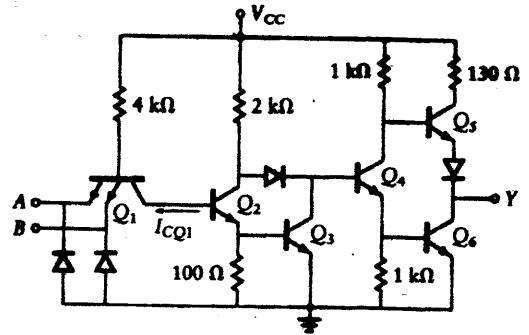


Figure P15.8

$Q_1$  &  $Q_2$  are as in usual TTL NAND.

A & B must both be "high" for  $I_{CQ1}$  to be "-".

If  $I_{CQ1}$  is "-",  $Q_2$  is "on", pulling base of  $Q_3$  to saturation (0.7-0.8V)

If  $Q_3$  is "on", the base of  $Q_4$  is 0.2V so  $Q_4$  is off.

Thus,  $Q_6$  base is at ground and base of  $Q_5$  is pulled up.

The output "1."

In the other 3 cases,  $I_{CQ1}$  is "+",  $Q_2$  is off,  $Q_3$  is off, the base of  $Q_4$  is pulled up through the 2kΩ resistor and diode. Since  $Q_4$  is on, the base of  $Q_5$  is pulled up and the voltage on the base of  $Q_5$  drops below the voltage necessary to turn it on.  $Q_4$ ,  $Q_5$  and  $Q_6$  form the usual "totem pole" output stage of a TTL circuit.

CMOS circuit:  $Q_1, Q_2, Q_3$  and  $Q_4$  perform the logic.  $Q_5$  and  $Q_6$  form an inverter.  $Q_7$  and  $Q_8$  make another inverter. So the output is the same as the drain of  $Q_4$ .  
Switch representation of  $Q_1, Q_2, Q_3, Q_4$ :

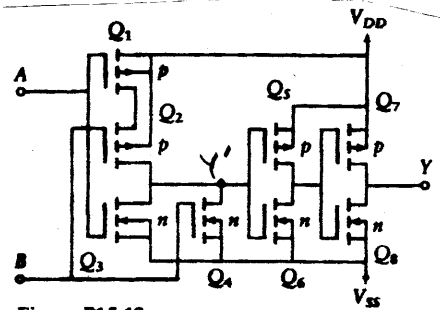
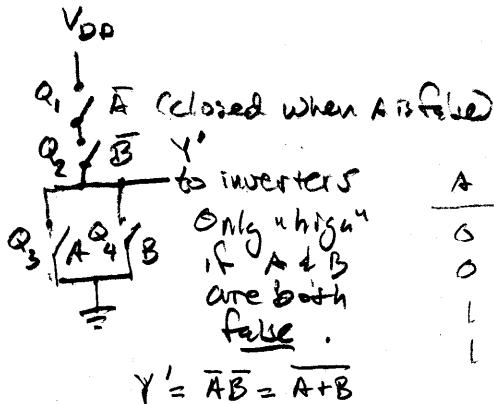


Figure P15.10



A	B	$Q_1$	$Q_2$	$Q_3$	$Q_4$	$Y'$	$Q_6$	$Q_7$	Y
0	0	N	N	F	F	1	F	N	1
0	1	N	F	F	F	0	N	F	0
1	0	F	N	F	F	0	N	F	0
1	1	F	F	N	N	0	N	F	0

Output is "NOR"