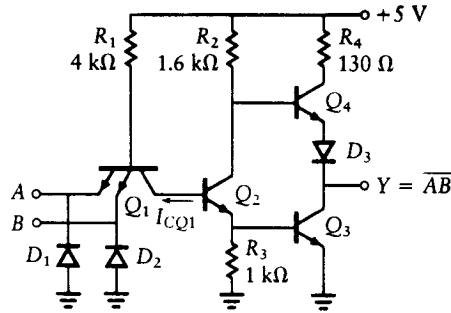


**Figure 15.9**  
Two-input TTL  
NAND gate (active  
pull-up).



(a) Schematic

A	B	$I_{CQ1}$	$Q_2$	$Q_3$	$Q_4$	Y
0	0	+	OFF	OFF	ON	1
0	1	+	OFF	OFF	ON	1
1	0	+	OFF	OFF	ON	1
1	1	-	ON	ON	OFF	0

(b) Function table

Example →  
Problem →

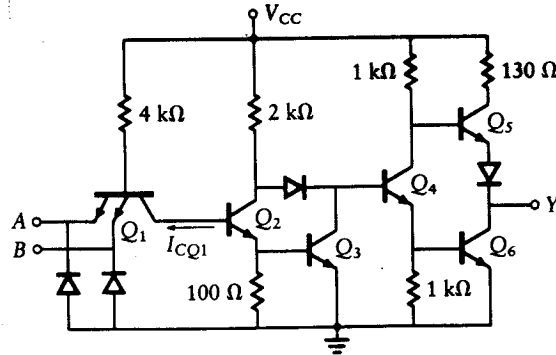
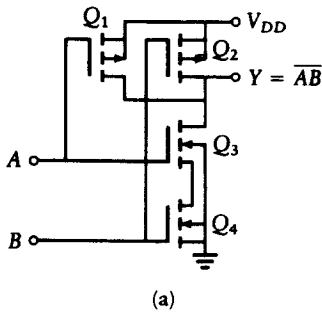


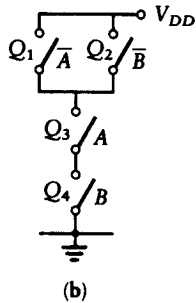
Figure P15.8

Determine the status of each transistor and prepare a function table for the TTL circuit  
*Q2 - Q6 also  $I_{CQ1}$  + or -*

$Q_1, Q_2 = p$ -channel  
 $Q_3, Q_4 = n$ -channel



(a)



(b)

A	B	$Q_1$	$Q_2$	$Q_3$	$Q_4$	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

(c)

**Figure 15.18**  
Two-input CMOS  
NAND gate.

Example →  
Problem →

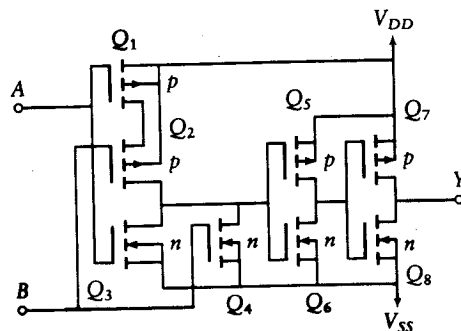


Figure P15.10

Determine the status of each FET and prepare a function table for the CMOS circuit

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