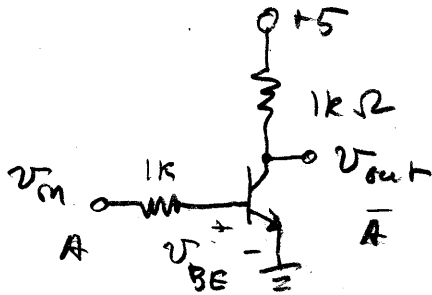


Logic circuits & how they work

(a) Evolution from RTL inverter to DTL NAND to TTL NAND (and Schottky TTL).

BJT as switch - cutoff or saturation (discussed earlier)



RTL inverter
a la lab

[see pulse performance plots]

For example (NOT TTL levels)

V_{in} low means $\approx 0.2V$

V_{in} high means $\geq 2V$

IF $V_{in} \approx 0.2V$, $V_{BE} < 0.5V$,

BJT is cut off, $V_{out} = 5V$

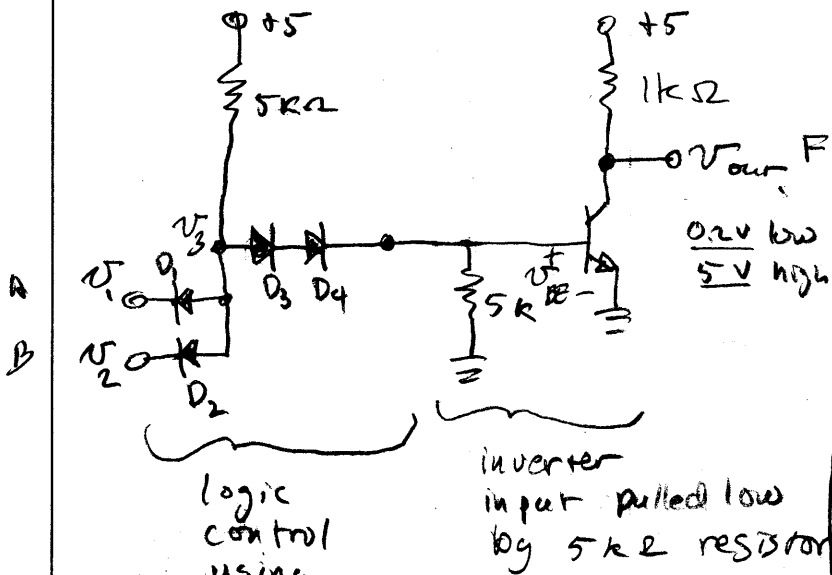
IF $V_{in} \geq 2V$, for reasonable R ,

transistor in saturation,

$V_{BE} \approx 0.8V$, $V_{out} \approx 0.2V$.

acts as logic inverter

DTL NAND gate uses diodes to form logic (Fig. 7.26 in text)



logic control using diodes

inverter input pulled low by 5k resistor

[assume fwd drop for diode is 0.7V]

D_3, D_4 are used to increase the turn-on threshold at the input due to their fwd voltage drop.

IF either V_1 or V_2 is at 0.2,

$V_B = 0.9V$, not

enough to turn BJT on (2 diode fwd drops + 0.5V required)

(E.g. if $V_1 = 0.2$, $V_2 = 5V$.

D_2 is reverse biased, but D_1 pulls BJT input down.)

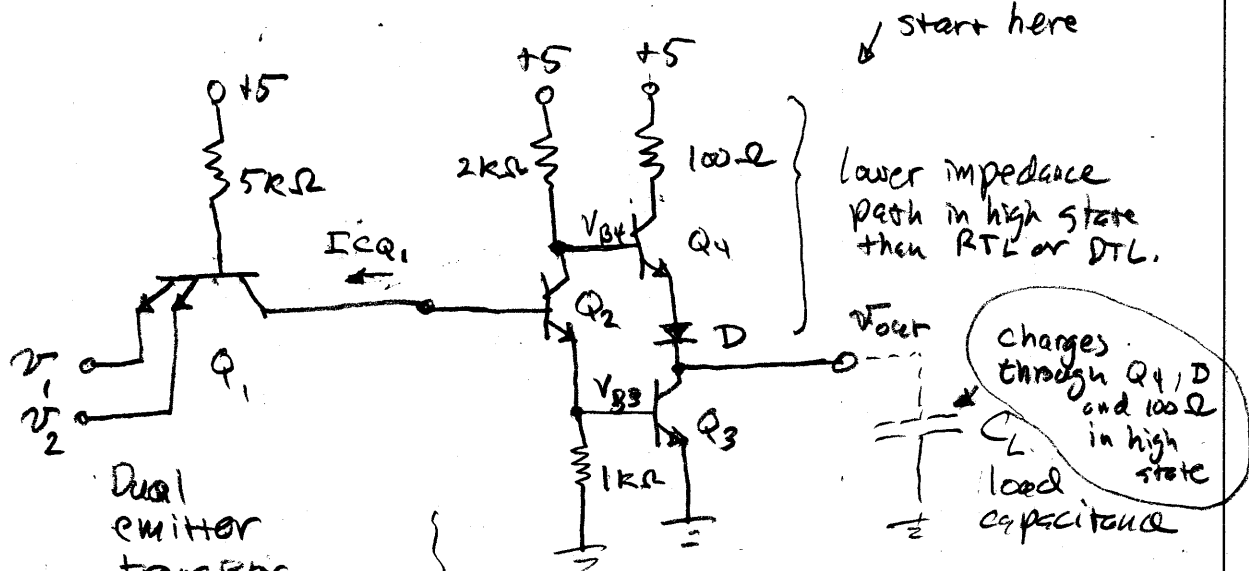
IF both V_1 and V_2 are +5V current flows through D_3 & D_4 to pull V_{BE} up to 0.8V and output goes low.

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

$F = \overline{AB}$
(NAND)

Improvement to make TTL NAND

→ To form pole output and transistor input replacing diodes (Fig. 7.32). Relation between v_{out}, v_1, v_2 is the same.
 Gives more drive current in the high state and faster response.



Dual emitter transistor replaces diode logic in DTL

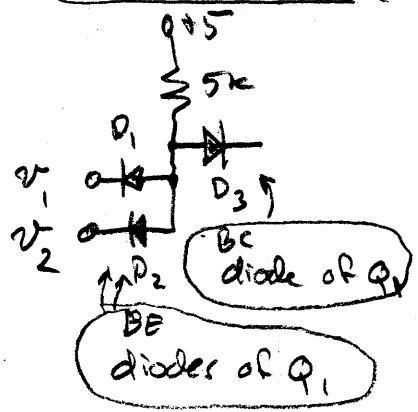
Totem pole output stage

Q_2 controls Q_4 and Q_3
 Q_2 off: Q_4 on, Q_3 off.
 ⇒ output high

Q_2 on:

$V_{CE2} = 0.2$ (saturation)
 $V_{B3} = 0.8$ (saturation)
 $V_{B4} = V_{C2} = 1.0V$
 $V_{out} = 0.2V$ (V_{CE2}) { output }
 The forward voltage drop across D is big enough to keep $V_{BE4} < 0.5V$ (off)
 $V_{BE4} + V_D = 1 - 0.2 = 0.8V$
 < sum of cut-in voltage.

Note the parallel (to DTL)



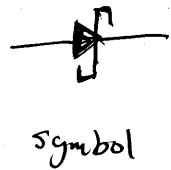
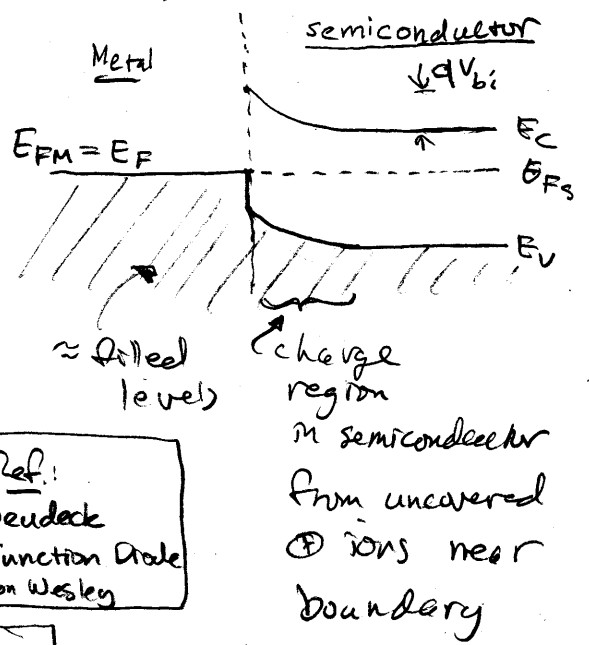
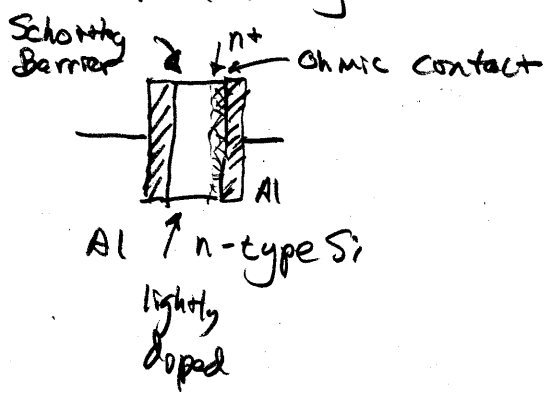
BJT provides current gain, an advantage over DTL.
 Note an conventional "reverse active" mode when v_1 and v_2 are both high.

v_1 or v_2 low ⇒ $I_{CQ1} > 0$, Q_2 off ⇒ output high
 v_1 and v_2 high ⇒ $I_{CQ1} < 0$, Q_2 on ⇒ output low ⇒ $Y = \bar{A} + \bar{B} = \overline{AB}$
 (see prob. handout)

Saturation may lead to long storage time, slowing BJT "off" transition (base region flooded with minority carriers, slowly diffuse out of BC depletion region).

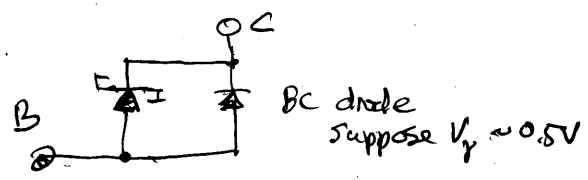
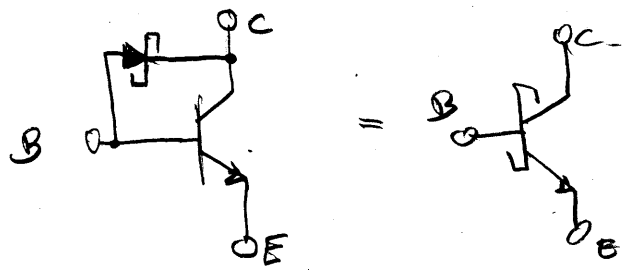
Prevent saturation with Schottky diode

- Metal-semiconductor junction - majority carrier device.
- Forward voltage drop 0.4 V rather than 0.7.
- use to prevent BJT base-collector diode from being forward biased, prevent saturation.



Ref:
G. Neudeck
PN Junction Diode
Addison Wesley

BJT with Schottky diode clamp



$V_{BC} \leq 0.4V < V_d$
BC diode never fully "on"
 $V_{CE} \geq 0.4V$ (if $V_{BE} = 0.8V$)

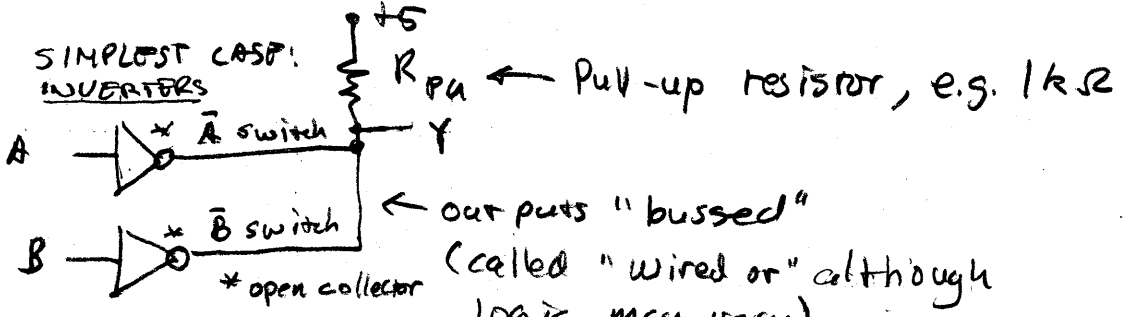
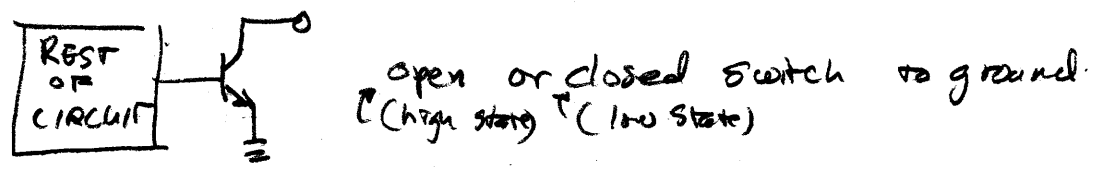
(Schottky TTL circuit - slightly different. See text.)

Forward bias reduces the net field, raising the E_c level in the bulk, more electrons get over from semiconductor there is a depletion region, but there are no minority carriers.

For ohmic contacts, use heavy doping, get tunneling through a narrow barrier (E_F within $3kT$ of E_c for degenerate semiconductor)

TTL CIRCUIT MODIFICATIONS TO ALLOW USE WITH DATA BUS - OUTPUT INTERCONNECTION

OPEN COLLECTOR OUTPUT:



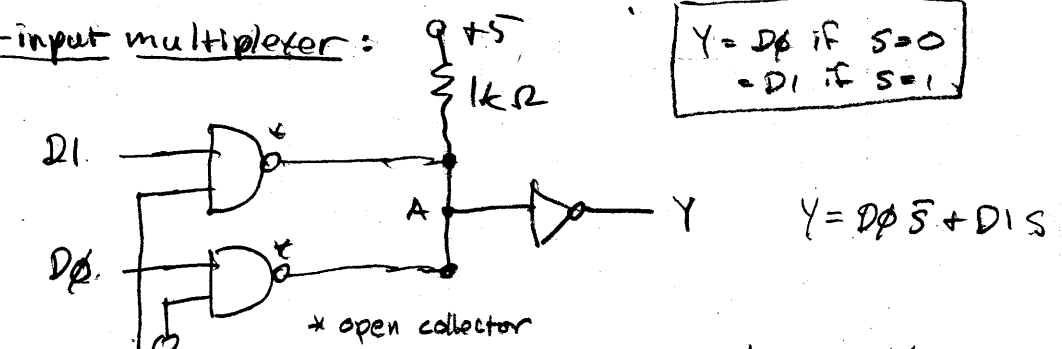
A	B	"SWITCHED"		Y (with pull-up)
		\bar{A}	\bar{B}	
L	L	OPEN	OPEN	H
L	H	OPEN	CLOSED	L
H	L	CLOSED	OPEN	L
H	H	CLOSED	CLOSED	L

$Y = \overline{A+B}$

Advantage: Simple

Disadvantage: can be slow, depending on R value.

Two-input multiplexer:



S	D1	D0	A	Y
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

$Y = D_0$ (for S=0)
 $Y = D_1$ (for S=1)

Simplified logic table

S	D1	D0	Y
0	x	0	0
0	x	1	1
1	0	x	0
1	1	x	1

x = "don't care"

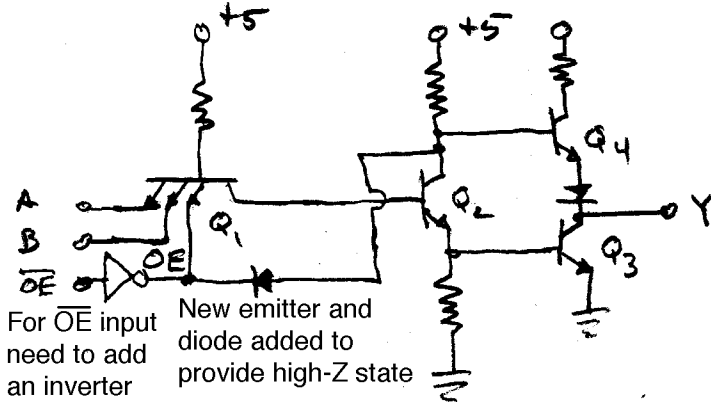
Tri-state output :

3 possibilities: H, L, high impedance ("Z")

- Better way to share bus lines - active pull-up in high state, no external pull-up required.

TTL circuit modification:

OE = output enable



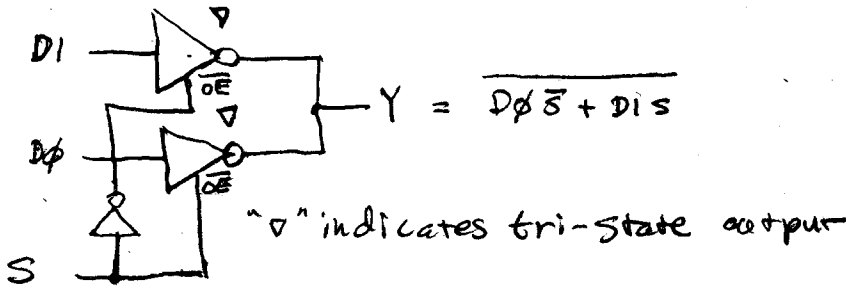
If OE is low, Q₁ pulls the base of Q₂ low, turning it off. The OE connection through the diode pulls the base of Q₄ low, turning it off. Since Q₂ is off, the base of Q₃ is at ground, so Q₃ is off. Thus the Y output is floating. ⇒ high impedance state.

0 = low, 1 = high

OE	OE	A	B	Y
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	x	x	High Impedance ("Z")

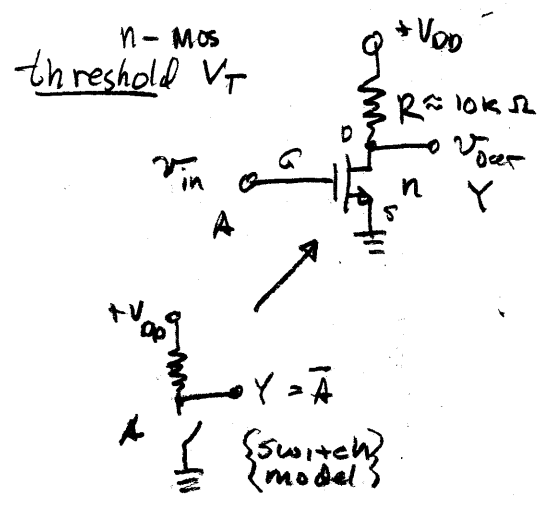
If oe is high, it has no further effect on circuit operation, as you can check.

Two-input multiplexer:



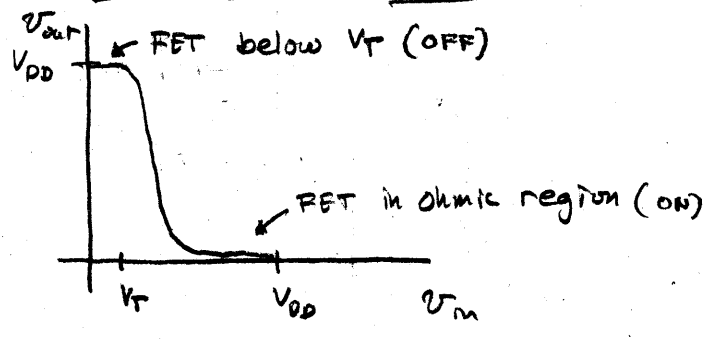
n-MOS and p-MOS transistors as switches and CMOS inverter

(a) Enhancement mode MOSFET as inverter:



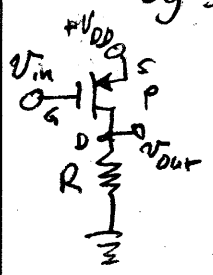
See text, Fig. 8.23

Approx. transfer characteristics:

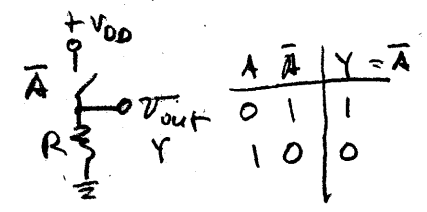


so if we use logic levels with Low < VT and High ≈ VDD, this is an inverter. Model MOSFET as open switch with Vin = Low and closed switch (although with non-negligible resistance) with Vin = High.

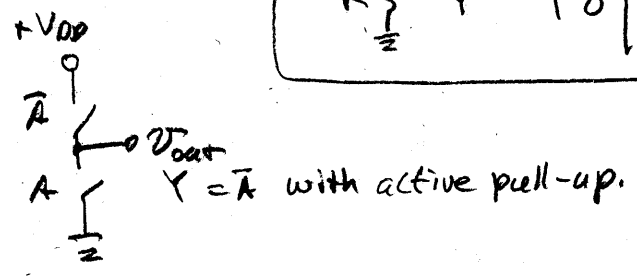
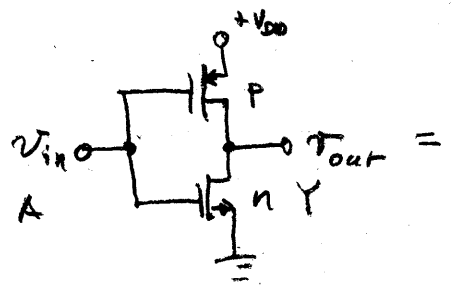
(b) By symmetry,



p-MOS with source hooked to +VDD and drain through R to ground would be open switch with Vin = High, closed switch (with non-negligible R) with Vin = Low. The switch is closed to +VDD so output would be high with input low:



(c) CMOS inverter



A	n-MOS	p-MOS	Y
L	OFF	ON	H
H	ON	OFF	L

(Very simple integrated circuit structure - See Text, Fig. 8.36)

→ See problem set for CMOS NAND example.