Logic Circuits II

Physics 116B, rev. 2/28/11

D. Pellett
Outline

• Emitter-Coupled Logic (ECL) example from Bobrow, Ch. 7

• Logic family comparisons
  • Interconnections, “dos and don’ts”
  • More recent developments

• Transmission Lines and Fast Logic Including ECL
  • Short pulses and transmission lines - quick overview
  • High bandwidth Oscilloscope Probes
  • Using ECL to drive transmission lines
  • High bandwidth oscilloscope probes
  • ECL and Nuclear Instrumentation Module (NIM) logic
Emitter Coupled Logic (ECL)

- ECL circuits are fast (1 ns delays typical) because they avoid saturation
- Can drive low impedance loads such as 50 Ω coaxial cables
- May have complimentary outputs to drive pairs of lines differentially (strip lines, twisted pairs, etc.)
- Because BJTs remain in active region, power dissipation significantly higher than TTL, low packing density on chip
- Circuit based on differential amplifier with non-inverting input connected to reference voltage, one BJT cut off and the other in active region
- Supply voltage and logic levels typically <0.
- Emitter follower outputs
  - May have “open emitter” output
Basic ECL Inverter Concept

Differential Amplifier

- Design so $Q_1$ active, $Q_2$ off when $V_{in}$ high,
- opposite w/$V_{in}$ low
- Determine logic levels next

NOTE: Circuit based on Fig. 7.43 in Bobrow
Commercial circuits differ in $V_{ref}$, $V_{EE}$ and BJT $V_{BE}(active)$ so actual ECL levels are different.
• Assume $V_{in}$ low so $Q_1$ off and $Q_2$ in active region

• $V_{BE2} = 0.7$ V so $V_E = -1.7$ V

• Since $Q_1$ off, $V_{C1} \approx 0$ V, so $V_0 = -0.7$ V (high logic state).

Note $Q_3$ is in active region with $V_{BE3} = 0.7$ V and $V_C = 0$ V: $V_{CE3} = 0.7$ V (> 0.2 V)

• Voltage drop across $R_1$ is negligible: $I_{E3} = (5-0.7)V/1.2$ kΩ = 3.6 mA $\rightarrow I_{B3} \approx 36$ µA, $I_{B3} R_1 = 10$ mV.
Find Low State Output Voltage

-0.82 V

Active

Off

-1.4 V

High -0.7 V

V_in

Q_1

Q_2

Q_3

V_o Low -1.52 V

-1V

-0.82 V

-1.52 V

-1.4 V

-5V

-1.2 kΩ

R_1 275Ω

R_2 300Ω

Emitter follower

• Assume V_{in} high and Q_1 in active region

• V_{BE1} = 0.7 V so V_E = -1.4 V. → V_{BE2} = 0.4 V so Q_2 off

• I_E = I_{E1} = (-1.4 -(-5))V/1.2 kΩ = 3.0 mA

• V_{C1} = V_{B3} ≈ -(3.0 mA)(275 Ω) = -0.82 V → V_o = -1.52 V

(low state output voltage, < -1.2 so low OK at input)
• Adding $Q_0$ in parallel with $Q_1$ produces a NOR function at $Q_3$ emitter.

• Adding an emitter follower connected to collector of $Q_2$ produces the complement of the function, an OR.
• BJT $V_{BE} = 0.8 - 0.9\, \text{V}$ for active region, $V_{BB} = -1.35\, \text{V}$, $V_{EE} = -5.2\, \text{V}$

• Logic levels are $-0.9\, \text{V}$ and $-1.75\, \text{V}$ (nominal)

• Note open emitter outputs
**Quad 2-Input NOR**

**MC10H102**

**Quad 2-Input NOR Gate**

The MC10H102 is a quad 2-input NOR gate. The MC10H102 provides one gate with OR/NOR outputs. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power–supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 25 mW/Gate (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

**LOGIC DIAGRAM**

<table>
<thead>
<tr>
<th>PIN</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC1</td>
</tr>
<tr>
<td>2</td>
<td>VCC2</td>
</tr>
<tr>
<td>3</td>
<td>G1</td>
</tr>
<tr>
<td>4</td>
<td>G2</td>
</tr>
<tr>
<td>5</td>
<td>G3</td>
</tr>
<tr>
<td>6</td>
<td>G4</td>
</tr>
<tr>
<td>7</td>
<td>IN1</td>
</tr>
<tr>
<td>8</td>
<td>IN2</td>
</tr>
<tr>
<td>9</td>
<td>IN3</td>
</tr>
<tr>
<td>10</td>
<td>IN4</td>
</tr>
<tr>
<td>11</td>
<td>OUT1</td>
</tr>
<tr>
<td>12</td>
<td>OUT2</td>
</tr>
<tr>
<td>13</td>
<td>OUT3</td>
</tr>
<tr>
<td>14</td>
<td>OUT4</td>
</tr>
</tbody>
</table>

VCC1 = PIN 1  
VCC2 = PIN 16  
VEE = PIN 8

**MARKING DIAGRAMS**

- **CDIP–16 L SUFFIX**  
  CASE 620  
  MC10H102L  
  AWLYYWW  
  1

- **PDIP–16 P SUFFIX**  
  CASE 648  
  MC10H102P  
  AWLYYWW  
  1

- **PLCC–20 FN SUFFIX**  
  CASE 775  
  10H102  
  AWLYYWW

**MARKING**

- A = Assembly Location  
- WL = Wafer Lot  
- YY = Year  
- WW = Work Week

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# MECL NOR Specifications

## MC10H102

### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{EE})</td>
<td>Power Supply ((V_{CC} = 0))</td>
<td>–8.0 to 0</td>
<td>Vdc</td>
</tr>
<tr>
<td>(V_I)</td>
<td>Input Voltage ((V_{CC} = 0))</td>
<td>0 to (V_{EE})</td>
<td>Vdc</td>
</tr>
<tr>
<td>(I_{out})</td>
<td>Output Current – Continuous</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>– Surge</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>(T_A)</td>
<td>Operating Temperature Range</td>
<td>0 to +75</td>
<td>°C</td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>Storage Temperature Range</td>
<td>–55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>– Ceramic</td>
<td>–55 to +165</td>
<td>°C</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS (\(V_{EE} = -5.2\) V ±5%) (See Note 1.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>0°C</th>
<th>25°C</th>
<th>75°C</th>
<th>Unit</th>
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<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>(I_E)</td>
<td>Power Supply Current</td>
<td>–</td>
<td>29</td>
<td>–</td>
<td>26</td>
</tr>
<tr>
<td>(I_{inH})</td>
<td>Input Current High</td>
<td>–</td>
<td>425</td>
<td>–</td>
<td>265</td>
</tr>
<tr>
<td>(I_{inL})</td>
<td>Input Current Low</td>
<td>0.5</td>
<td>–</td>
<td>0.5</td>
<td>–</td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>High Output Voltage</td>
<td>–1.02</td>
<td>–0.84</td>
<td>–0.98</td>
<td>–0.81</td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Low Output Voltage</td>
<td>–1.95</td>
<td>–1.63</td>
<td>–1.95</td>
<td>–1.63</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>High Input Voltage</td>
<td>–1.17</td>
<td>–0.84</td>
<td>–1.13</td>
<td>–0.81</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Low Input Voltage</td>
<td>–1.95</td>
<td>–1.48</td>
<td>–1.95</td>
<td>–1.48</td>
</tr>
</tbody>
</table>

### AC PARAMETERS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{pd})</td>
<td>Propagation Delay</td>
<td>0.4</td>
</tr>
<tr>
<td>(t_r)</td>
<td>Rise Time</td>
<td>0.5</td>
</tr>
<tr>
<td>(t_f)</td>
<td>Fall Time</td>
<td>0.5</td>
</tr>
</tbody>
</table>

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts.

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Logic Family Comparisons

- See Tables 12.5 and 12.6 in Bobrow, Tables 9.1 and 9.2 in Horowitz and Hill

- Important families: TTL, STTL, LSTTL, CMOS, HC, HCT, ECL
  - Important parameters: pulse delay, power per gate, logic level ranges, supply voltages, fanout
  - Incompatibilities of CMOS and HC with TTL high output

- See also later slides from the Texas Instruments Logic Selection Guide (2005)
Logic Family Comparisons

- The slide shown in class is available on SmartSite
Some Precautions

• TTL –
  • Inputs normally float “high” but if you desire high state connect to \( V_{CC} \) for noise immunity
  • Bypass \( V_{CC} \) to ground frequently near or at the chips with 0.01 \( \mu \)F – 0.1 \( \mu \)F capacitors to prevent glitches due to switching spikes on the supply lines.

• CMOS –
  • Note that TTL outputs are not high enough for normal CMOS inputs in high state – can remedy with pull-up resistor to \( V_{CC} \).
  • Connect all CMOS inputs to definite logic levels. Otherwise input can float to a voltage where pMOS and nMOS FETs are conducting leading to short between \( V_{SS} \) and \( V_{DD} \).
Welcome to the World of TI Logic

Recent Logic Families

3.3 V Logic
- AHC
- LV
- ALVT
- LVT
- ALVC
- LV-A
- AUP
- LVC
- CBTLV

1.8 V Logic
- LVC
- AVC
- AUP
- ALVC
- AUC

1.5 V Logic
- AUP
- AUC

1.2 V Logic
- AUC
- AUP

0.8 V Logic
- AUC

Specialty
- GTLP
- GTL
- BTL
- SSTL
- VME
- ETL

5+ V Logic
- LV-A
- CBT
- AC/ACT
- HC/HCT
- CD4000
- FCT
- TTL
- LS
- AHC
- AHCT
- S
- ABT
- ALS
- BCT

Harris now TI
Cypress now TI
Product Life Cycle

TI remains committed to be the last supplier in the older families.
Family Performance Positioning

Optimized $V_{cc}$
- 5 V
- 3.3 V
- 2.5 V
- 1.8 V

$\textbf{IoL Drive (mA)}$
- 100
- 64
- 24
- 8

$\textbf{Speed - max } t_{pd} \text{ (ns)}$
- 5
- 10
- 15
- 20

$\textbf{ABT}$ Advanced BiCMOS Technology
$\textbf{AC/T}$ Advanced CMOS
$\textbf{AHC/T}$ Advanced High Speed CMOS
$\textbf{ALVC}$ Advanced Low Voltage CMOS
$\textbf{ALVT}$ Advanced Low Voltage BiCMOS
$\textbf{AUC}$ Advanced Ultra Low Voltage CMOS
$\textbf{AUP}$ Advanced Ultra Low Power CMOS
$\textbf{AVC}$ Advanced Very Low Voltage CMOS
$\textbf{BCT}$ BiCMOS Technology
$\textbf{FCT}$ Fast CMOS Technology
$\textbf{GTLP}$ Gunning Transceiver Logic Plus
$\textbf{HC/T}$ High Speed CMOS
$\textbf{LV}$ Low Voltage HCMOS
$\textbf{LVC}$ Low Voltage CMOS
$\textbf{LVT}$ Low Voltage BiCMOS Technology

LOGIC SELECTION GUIDE
FIRST HALF 2005
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http://www.ti.com/sc/logic
IC Basics
Comparison of Switching Standards

<table>
<thead>
<tr>
<th>Voltage Type</th>
<th>Standard</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-V TTL</td>
<td>ABT, AHCT, HCT, ACT, Bipolar</td>
<td></td>
</tr>
<tr>
<td>5-V CMOS</td>
<td>Rail-to-Rail 5 V HC, AHC, AC, LV-A</td>
<td></td>
</tr>
<tr>
<td>3.3-V LVTTL</td>
<td>LVT, LVC, ALVC AUP, LV-A, ALVT</td>
<td></td>
</tr>
<tr>
<td>2.5-V CMOS</td>
<td>AUC, AUP, AVC, ALVC, LVC, ALVT</td>
<td></td>
</tr>
<tr>
<td>1.8-V CMOS</td>
<td>AUC, AUP, AVC, ALVC, LVC, LVC</td>
<td></td>
</tr>
</tbody>
</table>

- **5-V TTL**: 5V power, 0-5V Logic swing
- **5-V CMOS**: 5V power, ±5V Logic swing
- **3.3-V LVTTL**: 3.3V power, ±1.65V Logic swing
- **2.5-V CMOS**: 2.5V power, ±1.25V Logic swing
- **1.8-V CMOS**: 1.8V power, ±0.9V Logic swing

<table>
<thead>
<tr>
<th>Logic Levels</th>
<th>5TTL</th>
<th>5CMOS</th>
<th>3LVTTL</th>
<th>2.5CMOS</th>
<th>1.8CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_High</td>
<td>Yes</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
</tr>
<tr>
<td>V_Low</td>
<td>No</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
<td>Yes*</td>
</tr>
</tbody>
</table>

* Requires V_High Tolerance
What is Little Logic?
Single Gate/Dual Gate/Triple Gate

Principle

Quad-Gate
14-pin TSSOP
33.66 mm²

Single-Gate
5-pin YEA
1.26 mm²
Up to 96% less space

Dual-Gate
8-pin DCU
11.8 mm²
Up to 35% less space

Naming

SN74LVC 1G xx YEP R

Tape & Reel
R = 3000 piece
T = 250 piece

Package Type
YEP = NanoStar™ (230μ)
YZP = NanoFree™ (230μ)
DCK = SC-70
DBV = SOT-23
DCU = US-8
DCT = SM-8

Logic Function
xx

Gate Count
1G - Single Gate
2G - Dual Gate
3G - Triple Gate

Product Family
AHC/T, AUC, AUP, CBT, LVC

Standard Prefix
Pulses and Transmission Lines

Transmission lines (more in 116c)

Coaxial cable

Parallel conductors

Twisted pair

Strip line

Ground plane on backside of circuit board

Metal chassis

Wires have \( L, C \)

Pulse response:
- Overshoot
- Undershoot
- Ringing
- Cross talk
- Pickup

Random wires on proto-board not so much
Transmission Line Circuit Model

Lumped model of transmission line \((\text{Ideal, lossless})\)

\[ V_{in} \rightarrow \frac{L}{c} \rightarrow \frac{L}{c} \rightarrow \frac{L}{c} \rightarrow V_{out} \]

Distributed \{ inductance \ \frac{L}{\text{unit length}} \}
\{ capacitance \ \frac{C}{\text{unit length}} \}

Can show that a pulse travels as a wave.

For coaxial cable, (others similar)

\[ L = \frac{\mu}{2\pi} \ln \frac{b}{a} \]
\[ C = \frac{2\pi\varepsilon}{\ln \frac{b}{a}} \]

\[ v^2 = \frac{1}{LC} = \frac{1}{\mu\varepsilon} \leq C^2 \]

Characteristic impedance \[ Z_{ch} = \sqrt{\frac{1}{C}} = \frac{\frac{\mu}{2\pi}}{\sqrt{\frac{\ln \left(\frac{b}{a}\right)}{\ln \frac{b}{a}}}} \] (real)

(assume resistances and leakages "small")

If the line is terminated with \( R = Z_{ch} \), it appears to the pulser as if it were simply a resistor \( R \).

The resistor sees a delayed version of the original pulse.
Typical Characteristic Impedance Values
Other Transmission Line Advantages

$$Z_{ch} = 50 \, \Omega, \; 75 \, \Omega \text{ for common coax cables}$$
$$\approx 120 \, \Omega \text{ for wire over metal plate}$$
$$300 \, \Omega \text{ for TV "twin lead"}$$

Relatively low impedance.

Other advantages: reduction of pickup for external signals (interference, crosstalk).
Lots of Useful Information on Fast Pulse Techniques in MECL Handbook

Wire Over Ground
Figure 3-4 shows the cross section of a wire over a ground. The characteristic impedance of the wire is

\[ Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{4h}{d} \right) \]

where \( \varepsilon_r \) is the effective dielectric constant surrounding the wire. The wire over a ground plane is most useful for breadboard layout and for backplane wiring. The characteristic impedance of a wire over a ground plane in the backplane is about 120 ohms, although this may vary as much as ±40% depending on the distance from the plane, proximity of adjacent wires, and the configuration of the ground.

Microstrip Lines
A microstrip line (Figure 3-5) is a strip conductor (signal line) separated from a ground plane by a dielectric. If the thickness, width of the line, and the distance

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http://onsemi.com

• Web link to download MECL Handbook (pdf):

http://www.onsemi.com/pub/Collateral/HB205-D.PDF
Pulse Response on “Open Wire”

3-1: Overshoot and Undershoot With an Open Wire Line

(a) Test Arrangement

(b) Ground Plane Not Used

(c) Ground Plane Added

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http://onsemi.com
ECL Driving 50 Ω Coaxial Cable

3-2: Matched Transmission Line Waveshapes

(a) Test Configuration

(b) Input and Output Waveforms

Vertical Scale = 400 mV/cm
Horizontal Scale = 10 ns/cm

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http://onsemi.com

Much Better!
ECL Differential Line Driver and Receiver

4-8: Twisted-Pair Line Driver and Receiver

4-9: 1/4 MC10115 Schematic

4-14: 50 Ft Twisted Pair Line with MECL 10K

Horizontal Scale = 5 ns/div.
Vertical Scale = 500 mV/div.
Oscilloscope Probes for Fast Signals in Action

Leading edge trigger circuit from Lab 13

74LS04 Hex Inverter
switching characteristics, $V_{CC} = 5\, \text{V}$, $T_A = 25\, ^\circ\text{C}$ (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>SN54S04</th>
<th>SN74S04</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A</td>
<td>Y</td>
<td>$R_L = 280, \Omega$, $C_L = 15, \text{pF}$</td>
<td>3</td>
<td>4.5</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>A</td>
<td>Y</td>
<td>$R_L = 280, \Omega$, $C_L = 50, \text{pF}$</td>
<td>4.5</td>
<td>ns</td>
</tr>
</tbody>
</table>

9 ns pulse width FWHM is in good agreement with 74LS04 specs
How Can Oscilloscope Probe Avoid Reflections In Transmitting Pulse?

- The “x10” probe has a parallel R and C compensated voltage divider network to reduce the capacitance seen by the external circuit.

- This decreases the rise time for a given source resistance (see Problem 1 on 2011 midterm).

- But with fast rise time pulses, one also needs to prevent reflections due to the unterminated transmission line.

- This is crucial when the rise time is comparable to the length of time it takes for a pulse to traverse the cable.

- Resistive wire in cable (“lossy transmission line”) and other features are provided in high bandwidth probes to absorb the energy which would otherwise be reflected, distorting the signal.

- A nice article on this subject is here:
  Secret world of oscilloscope probes
  (http://esvc000124.wic048u.server-web.com/links/THE%20SECRET%20WORLD%20OF%20PROBES%20OCT09.pdf)
AN INTRODUCTION TO NIM (From Fermilab web site)

The NIM standard (DOE/ER-0457), originally an acronym for Nuclear Instrumentation Methods, was established in 1964 for the nuclear and high energy physics communities. The goal of NIM was to promote a system that allows for interchangeability of modules. Even today experimenters use NIM modules to assemble a system which meets the specific requirements of their experiment.

Standard NIM modules are required to have a height of 8.75", and must have a width which is a multiple of 1.35". Modules with a width of 1.35" are referred to as single width modules and modules with a width of 2.7" are double width modules, etc. The NIM crate, or NIM bin, is designed for mounting in EIA 19" racks, providing slots for 12 single-width modules. The power supply, which is in general, detachable from the NIM bin, is required to deliver voltages of +6 V, -6 V, +12 V, -12 V, +24 V, and -24 V. The standard NIM power connectors and pinouts are shown in the Bin Connector Diagram, Module Connector Diagram, and Pin/Function Table. The LeCroy NIM bin and power supply, Model 1403, adhere to all NIM specifications.

The NIM standard also specifies three sets of logic levels. In fast-negative logic, usually referred to as NIM logic, logic levels are defined by current ranges. Since the standard also requires 50 W input/out impedances, these current ranges correspond to voltages of 0 V and -0.8 V for logic 0 and 1 respectively. Fast-negative logic circuitry can provide NIM signal with rise times of order 1 nsec. Slow-positive logic, is rarely used in fast-pulse electronics due to the slow rise times involved, and is not implemented in LeCroy modules. Specifications for ECL (emitter-coupled logic) voltage levels and interconnections have been added to the NIM standard at the request of LeCroy. The logic levels, header sizes, cable terminations, etc., is specified in the standard. The TTL logic system may be used in NIM modules, but is not specified in the NIM standard. LeCroy provides the Model 688AL and the Model 4616 for NIM/TTL and ECL/NIM/ECL level translations. LeCroy also provides the Model 4501A adaptor, which allows a NIM modules to be used in a CAMAC crate.

(From http://www-esd.fnal.gov/esd/catalog/intro/intronim.htm)

- ECL can be made to interoperate directly with NIM logic levels with suitable choice of offset ECL power supply voltages
Collider Detector at Fermilab (CDF) Control Room – Lots of fast pulses!

- Collecting data from high energy proton-antiproton collisions. But not all chips are microchips in this experiment (see foreground).

- Note NIM electronics bin in rack near back corner
Some CDF Control Room Electronics

- NIM Bin
- Some of the other bins are CAMAC bins
- Much custom electronics in use elsewhere in experiment, some “standard” (e.g. VME), some not
- Similar equipment is also in use in the Physics122 lab next door in Roessler