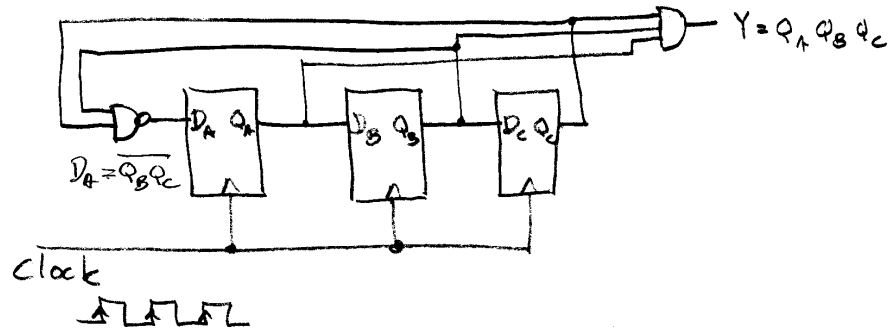
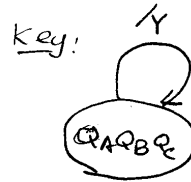
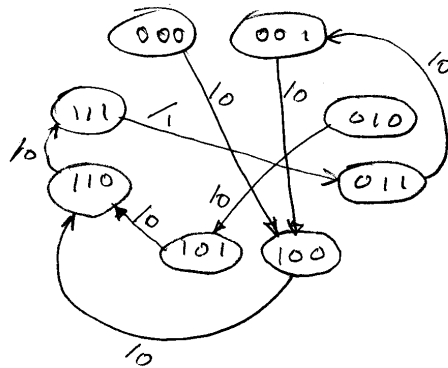


## Problem on glitches, maximum clock frequency

1. The complete state diagram is shown for the synchronous circuit below.
  - (a) If the circuit is started in the state 111, it follows a recurring sequence of states. Are there any transitions in this sequence which produce a glitch at the  $Y$  output? Explain why or why not.
  - (b) Calculate the maximum clock frequency using the parameters in Table 1.



State diagram



$$D_A = \overline{Q_B Q_C} \equiv \overline{Q_B} + \overline{Q_C}$$

$$Y = Q_A Q_B Q_C$$

Table 1: Chip Timing Specifications for Problem 4

Parameter	Maximum	Typical	Minimum
NAND propagation delay	15 ns	10 ns	-
Flip-flop propagation delay	30 ns	20 ns	-
Flip-flop setup time	-	-	25 ns
Flip-flop hold time	-	-	5 ns
Flip-flop clock pulse width	-	-	20 ns
Flip-flop clock frequency	30 MHz	-	-