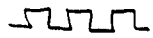
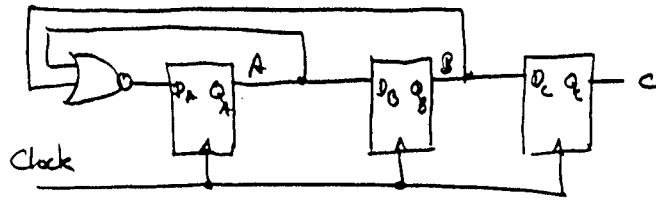


1.



- Determine the complete state diagram for the shift-register counter shown above.
- Indicate any stable, repetitive counting sequences.
- Is this ^{circuit} synchronous or asynchronous? Explain briefly.
- Calculate the maximum clock frequency for the circuit, given the following specifications:

	max.	typical	minimum
NOE propagation delay:	15 ns	10 ns	—
Flip-flop " " :	30 ns	20 ns	—
" setup time :	—	—	25 ns
" hold time :	—	—	0 ns
" clock pulse width:	—	—	20 ns
" clock frequency	30 MHz	—	—

2. Analyze the operation of the following circuit.

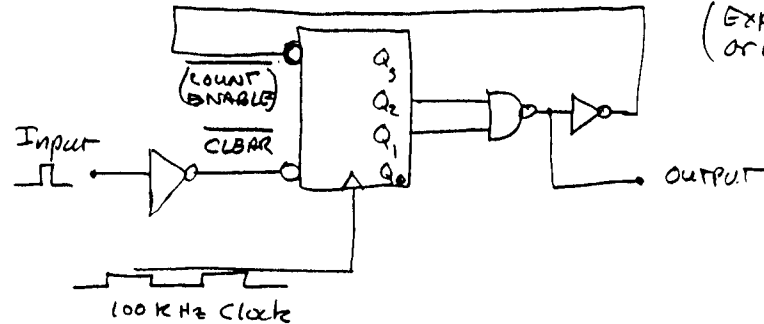
The box represents a 4-bit synchronous binary counter. The clock runs at a continuous 100 kHz rate. The CLEAR input is asynchronous.

- Suppose the input remains low for a long time. In what state will the counter eventually remain? What will be the state of the output?
- Now suppose a 1 μ s positive pulse arrives at the input (sufficient to reset the counter). What happens now? What is the minimum length of the output pulse? (Explain.)

(c) What happens if a second input pulse arrives while the output is high?

(d) Can there be "glitches" on the output pulse?

(Explain why or why not.)



* Assume the counter is initially reset to 0 when the power is first turned on.