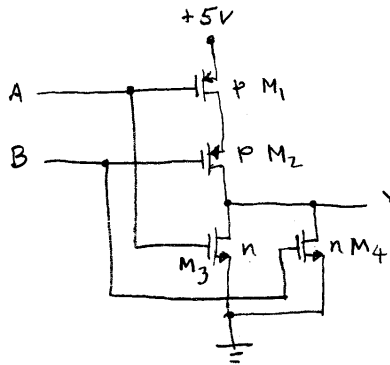


Physics 116B Winter 2007: Problem set 7

2/10/2006

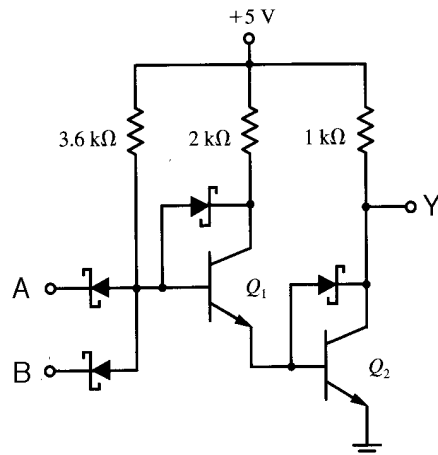


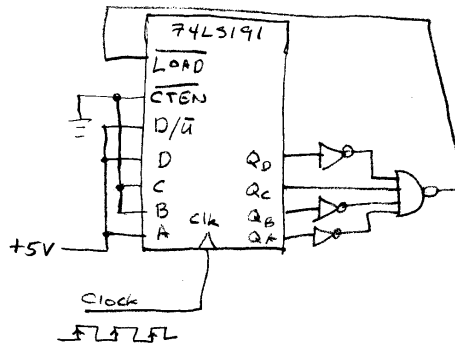
1. In the circuit above, the p-channel enhancement mode MOSFETs have $V_t = -1.5 \text{ V}$ and the n-channel enhancement mode MOSFETs have $V_t = 1.5 \text{ V}$. The logic levels are 5 V (H) or 0 V (L).

Make a truth table, specifying the state (“on” or “off”) of each MOSFET M_1 through M_4 as a function of A and B and the state of Y (H or L). From this, find the logical function performed by the circuit.

2. Another logic circuit is given below.

- (a) Are the diodes in the circuit p - n silicon junction diodes? If not, what kind of diodes are they?
- (b) What do they do to improve the performance of the circuit?
- (c) Assume the logic levels for this circuit are approximately 5 V (H) or 0 V (L). Make a truth table as a function of A and B specifying the states (“on” or “off”) of Q_1 and Q_2 and the state of Y (H or L).
- (d) Determine the logical function performed.





3. The circuit above is made with a 74LS191 synchronous binary up/down counter with asynchronous load (the datasheet for the counter is included with the information posted on the web with the Lab 16 writeup). After the clock is started, the counter eventually enters a repetitive sequence of states.
- Make a complete state diagram showing the repetitive sequence. Label each state with the decimal number corresponding to the state (Q_A is the least significant bit). Indicate any state transitions which are not synchronous with the clock.
 - Assume the clock period is much longer than the time for the asynchronous transition. What is the sequence of states immediately prior to the clock transitions?
 - In this sequence, are there any transitions which could produce glitches on the $\overline{\text{LOAD}}$ input? If so, which ones? What sort of problem could such a glitch cause for the circuit?